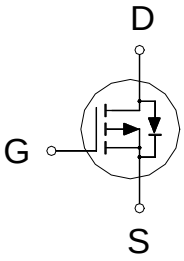
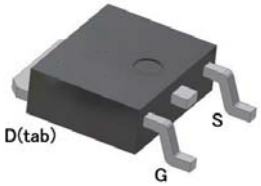
P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-30V
$R_{DSON\ (MAX.)}$	8mΩ
I_D	-70A





UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±25	V
Continuous Drain Current	T_C = 25 °C	I_D	-70	A
	T_C = 100 °C		-50	
Pulsed Drain Current[1]		I_{DM}	-150	
Avalanche Current		I_{AS}	-50	
Avalanche Energy	L = 0.1mH, I_D=-50A, R_G=25Ω	E_{AS}	125	mJ
Power Dissipation	T_C = 25 °C	P_D	62.5	W
	T_C = 100 °C		25	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

100% UIS testing in condition of V_D=-15V, L=0.1mH, V_G=-10V, I_L=-40A, Rated V_{DS}=-30V P-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		2	°C / W
Junction-to-Ambient[3]	$R_{\theta JA}$		50	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1.5	-2.5	-3.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±25V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24V, V_{GS} = 0V			-1	μA
		V_{DS} = -20V, V_{GS} = 0V, T_J = 125 °C			-10	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -10V	-70			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -10V, I_D = -25A		7	8	mΩ
		V_{GS} = -7V, I_D = -15A		8.5	12	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -25A		24		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -15V, f = 1MHz		2788		pF
Output Capacitance	C_{oss}			412		
Reverse Transfer Capacitance	C_{rss}			362		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz		3.3		Ω
Total Gate Charge[1,2]	Q_g	V_{DS} = -15V, V_{GS} = -10V, I_D = -25A		47.3		nC
Gate-Source Charge[1,2]	Q_{gs}			6		
Gate-Drain Charge[1,2]	Q_{gd}			9.1		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = -15V, I_D = -1A, V_{GS} = -10V, R_{GS} = 2.7Ω		18		nS
Rise Time[1,2]	t_r			26		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			22		
Fall Time[1,2]	t_f			75		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				-70	A
Pulsed Current[3]	I_{SM}				-150	
Forward Voltage[1]	V_{SD}	I_F = -24A, V_{GS} = 0V			-1.2	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100A / μS		50		nS
Reverse Recovery Charge	Q_{rr}			60		nC

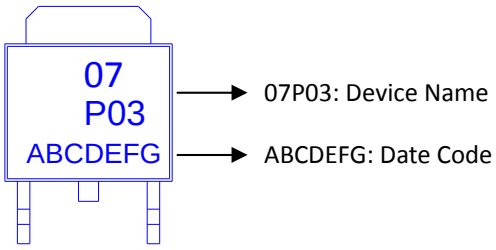
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

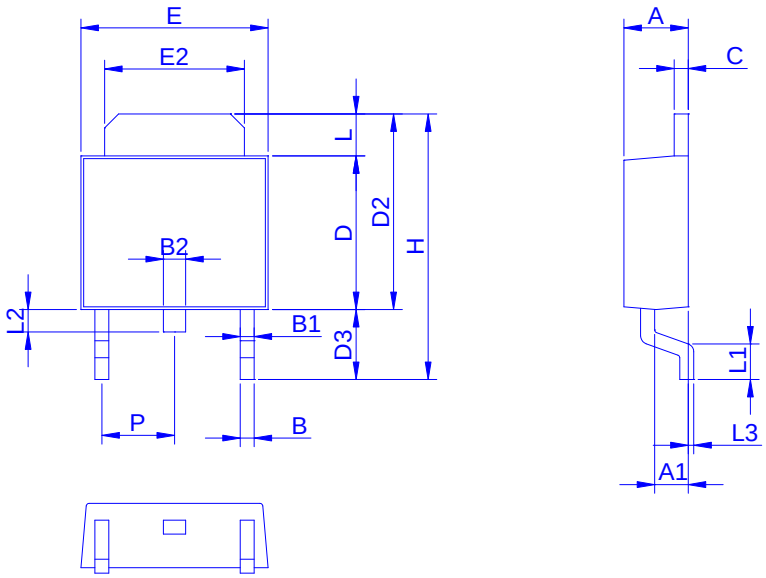
[3]Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: LB07P03D for DPAK (TO-252)

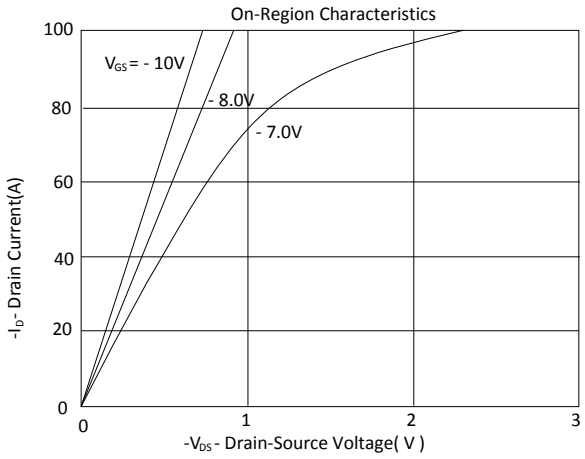


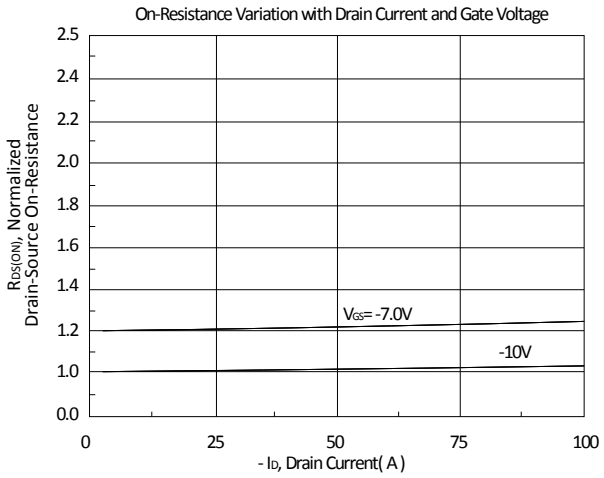
Outline Drawing

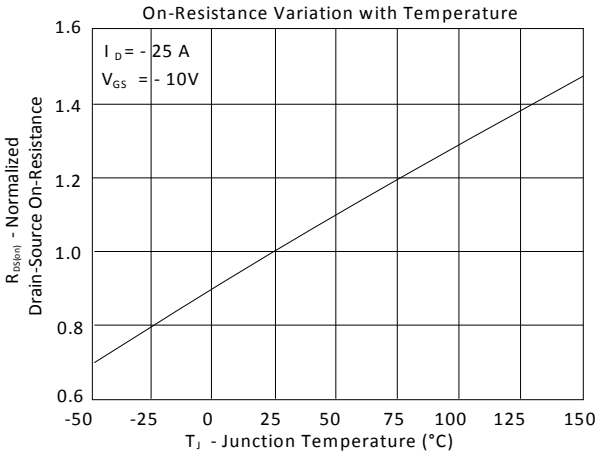


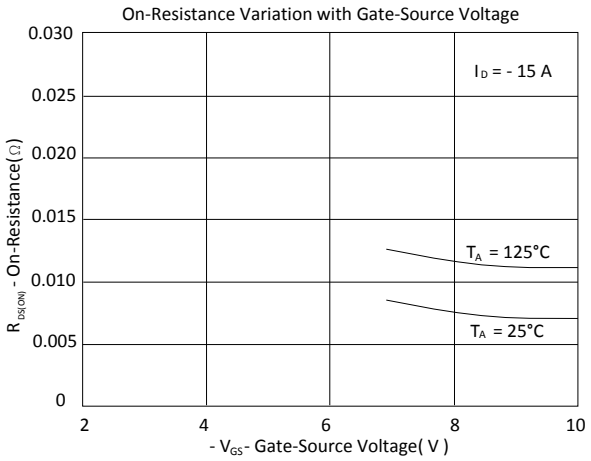
Dimension in mm

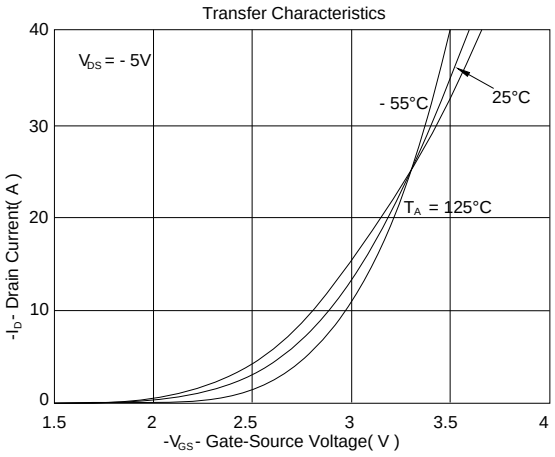
Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	0.95	0.30	0.40	0.60	0.40	5.30	6.70	2.20	6.40	4.80	9.20	0.89	0.90	0.50	0.00	2.10
Max.	2.50	1.30	0.85	0.94	1.00	0.60	6.20	7.30	3.00	6.70	5.45	10.15	1.70	1.65	1.10	0.30	2.50

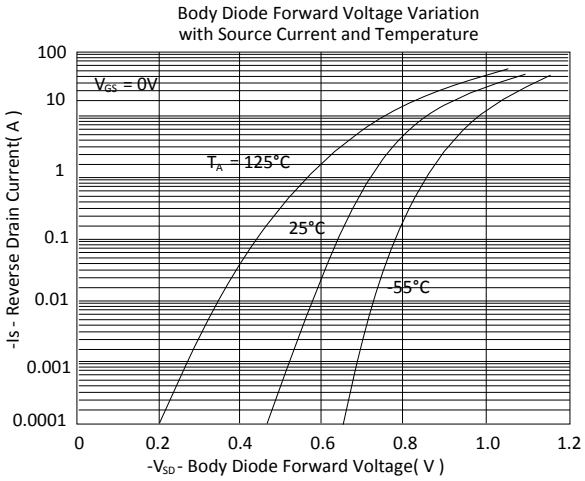

On-Region Characteristics
VGS = - 10V
- 8.0V
- 7.0V
-ID - Drain Current(A)
-VDS - Drain-Source Voltage(V)

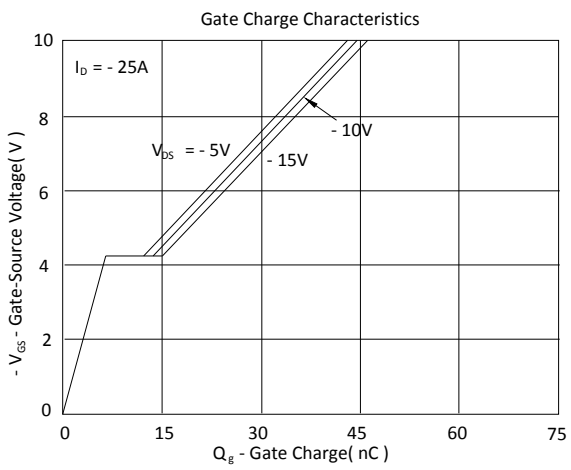

On-Resistance Variation with Drain Current and Gate Voltage
RDS(ON), Normalized
Drain-Source On-Resistance
VGS= -7.0V
-10V
- ID, Drain Current(A)

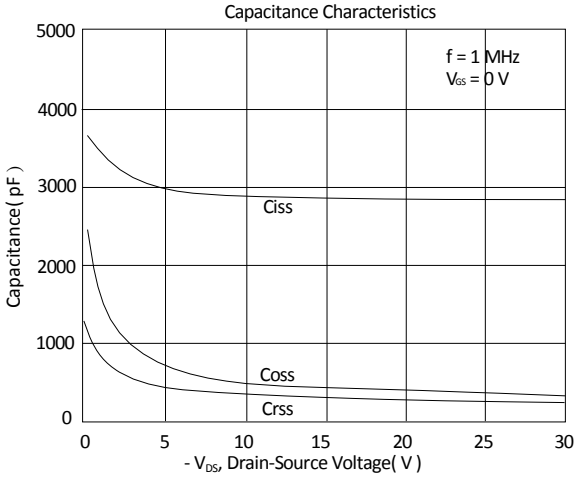

On-Resistance Variation with Temperature
I D = - 25 A
VGS = - 10V
RDS(on) - Normalized
Drain-Source On-Resistance
TJ - Junction Temperature (°C)

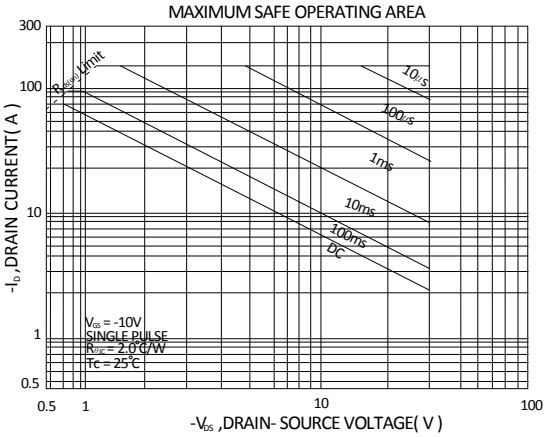

On-Resistance Variation with Gate-Source Voltage
I D = - 15 A
TA = 125°C
TA = 25°C
RDS(ON) - On-Resistance(Ω)
- VGS- Gate-Source Voltage(V)

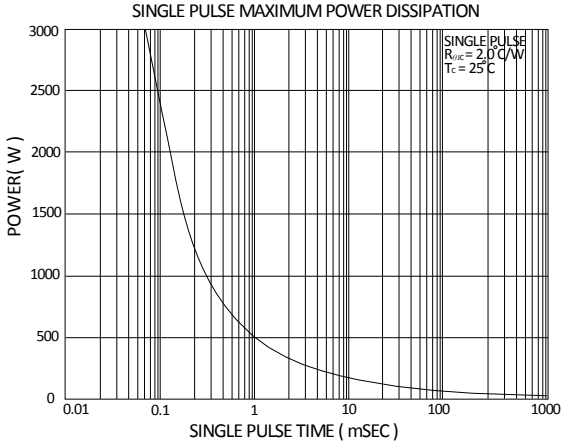

Transfer Characteristics
VDS = - 5V
- 55°C
25°C
TA = 125°C
-ID - Drain Current(A)
-VGS - Gate-Source Voltage(V)

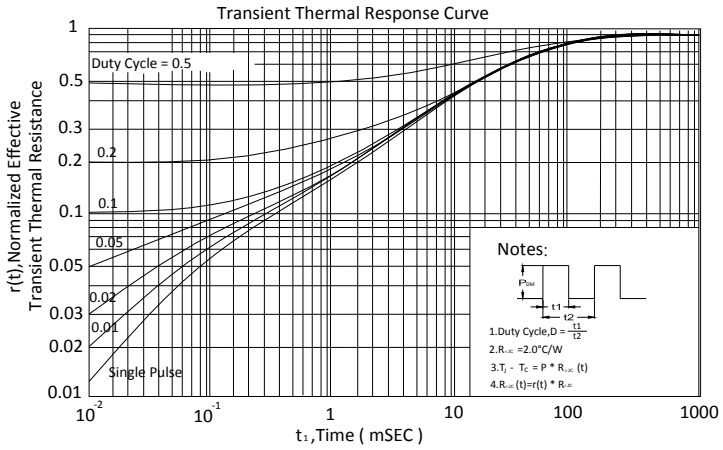

Body Diode Forward Voltage Variation
with Source Current and Temperature
VGS = 0V
TA = 125°C
25°C
-55°C
-Is - Reverse Drain Current(A)
-VSD - Body Diode Forward Voltage(V)


Gate Charge Characteristics
I_D = - 25A
V_{DS} = - 5V
- 10V
- 15V
- V_{GS} - Gate-Source Voltage(V)
Q_g - Gate Charge(nC)


Capacitance Characteristics
f = 1 MHz
V_{GS} = 0 V
Ciss
Coss
Crss
Capacitance(pF)
- V_{DS}, Drain-Source Voltage(V)


MAXIMUM SAFE OPERATING AREA
$R_{DS(on)}$ Limit
10μs
100μs
1ms
10ms
100ms
DC
V_{GS} = -10V
SINGLE PULSE
R_{thJC} = 2.0°C/W
Tc = 25°C
-I_D,DRAIN CURRENT(A)
-V_{DS} ,DRAIN- SOURCE VOLTAGE(V)


SINGLE PULSE MAXIMUM POWER DISSIPATION
SINGLE PULSE
R_{thJC} = 2.0°C/W
Tc = 25°C
POWER(W)
SINGLE PULSE TIME (mSEC)


Transient Thermal Response Curve
Duty Cycle = 0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
Notes:
1.Duty Cycle,D = t1/t2
2.R_{thJC} =2.0°C/W
3.T_J - T_C = P * R_{thJC} (t)
4.R_{thJC} (t)=r(t) * R_{thJC}
r(t),Normalized Effective Transient Thermal Resistance
t_1,Time (mSEC)