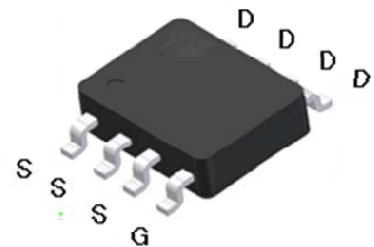


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	100V
R _{DS(on)} (MAX.)	12mΩ
I _D	12A



UIS, R_g 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current ³	T _A = 25 °C	I _D	12	A
	T _A = 100 °C		7.3	
Pulsed Drain Current ¹		I _{DM}	48	
Avalanche Current		I _{AS}	12	mJ
Avalanche Energy	L = 0.1mH, I _D =12A, R _G =25Ω	E _{AS}	7.2	
Repetitive Avalanche Energy ²	L = 0.05mH	E _{AR}	3.6	
Power Dissipation	T _A = 25 °C	P _D	2.5	W
	T _A = 100 °C		1	
Operating Junction & Storage Temperature Range		T _j , T _{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}		25	°C / W
Junction-to-Ambient	R _{θJA}		50	

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

³The maximum current rating is package limited.

ELECTRICAL CHARACTERISTICS (T_j = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	100			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.0	2.0	3.0	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80V, V _{GS} = 0V			1	μA
		V _{DS} = 70V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	12			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 10V, I _D = 12A		10	12	mΩ
		V _{GS} = 4.5V, I _D = 10A		13.5	17	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 12A		45		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 50V, f = 1MHz		2130		pF
Output Capacitance	C _{oss}			336		
Reverse Transfer Capacitance	C _{rss}			29		
Gate Resistance	R _g	V _{GS} = 15mV, V _{DS} = 0V, f = 1MHz		1.5		Ω
Total Gate Charge ^{1,2}	Q _g (V _{GS} =10V)	V _{DS} = 50V, V _{GS} = 10V, I _D = 12A		38		nC
	Q _g (V _{GS} =4.5V)			23		
Gate-Source Charge ^{1,2}	Q _{gs}			10		
Gate-Drain Charge ^{1,2}	Q _{gd}			8.2		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{DS} = 50V, I _D = 12A, V _{GS} = 10V, R _{GS} = 6Ω		6		nS
Rise Time ^{1,2}	t _r			10		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			8		
Fall Time ^{1,2}	t _f			25		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _c = 25 °C)						
Continuous Current	I _S				2.3	A
Pulsed Current ³	I _{SM}				9.2	
Forward Voltage ¹	V _{SD}	I _F = I _S , V _{GS} = 0V			1.2	V
Reverse Recovery Time	t _{rr}	I _F = 12A, dI _F /dt = 500A / μS		25		nS
Reverse Recovery Charge	Q _{rr}			120		nC

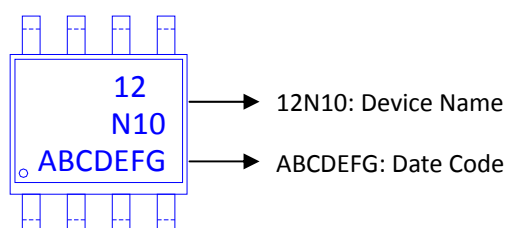
¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

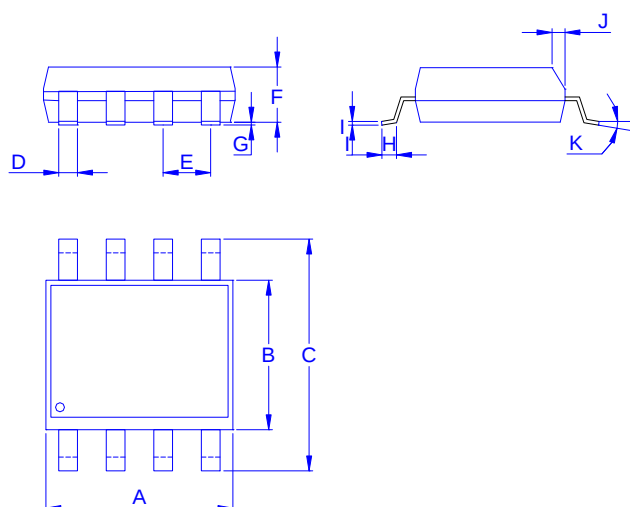
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: LB12N10H for SOP-8



Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°

TYPICAL CHARACTERISTICS

