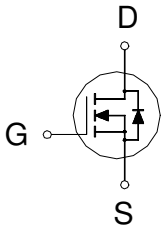
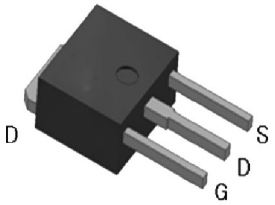
N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	80V
$R_{DSON\ (MAX.)}$	65mΩ
I_D	15A





UIS, 100% Tested

Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	15	A
	T_C = 100 °C		10	
Pulsed Drain Current[1]		I_{DM}	60	
Avalanche Current		I_{AS}	23	
Avalanche Energy	L = 0.1mH, ID=23A, RG=25Ω	E_{AS}	27	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	E_{AR}	13	
Power Dissipation	T_C = 25 °C	P_D	39	W
	T_C = 100 °C		15	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		3.2	°C / W
Junction-to-Ambient[3]	$R_{\theta JA}$		50	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	80			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.0	1.7	3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 64V, V_{GS} = 0V			1	μA
		V_{DS} = 60V, V_{GS} = 0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5V, V_{GS} = 10V	15			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 15A		55	65	mΩ
		V_{GS} = 5V, I_D = 10A		68	85	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 15A		12		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 30V, f = 1MHz		1110		pF
Output Capacitance	C_{oss}			60		
Reverse Transfer Capacitance	C_{rss}			51		
Total Gate Charge[1,2]	Q_g	V_{DS} = 40V, V_{GS} = 10V, I_D = 15A		15		nC
Gate-Source Charge[1,2]	Q_{gs}			1.7		
Gate-Drain Charge[1,2]	Q_{gd}			4.1		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = 40V, I_D = 1A, V_{GS} = 10V, R_{GS} = 6Ω		10		nS
Rise Time[1,2]	t_r			8		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			18		
Fall Time[1,2]	t_f			6		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				15	A
Pulsed Current[3]	I_{SM}				60	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			1.3	V
Reverse Recovery Time	t_{rr}	I_F = 10A, dI_F/dt = 100A / μS		120		nS
Reverse Recovery Charge	Q_{rr}			500		nC

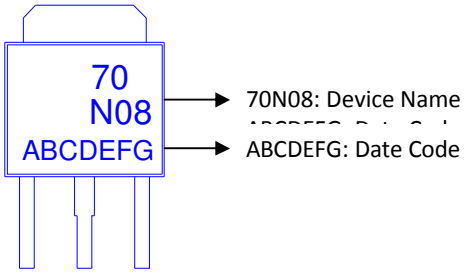
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

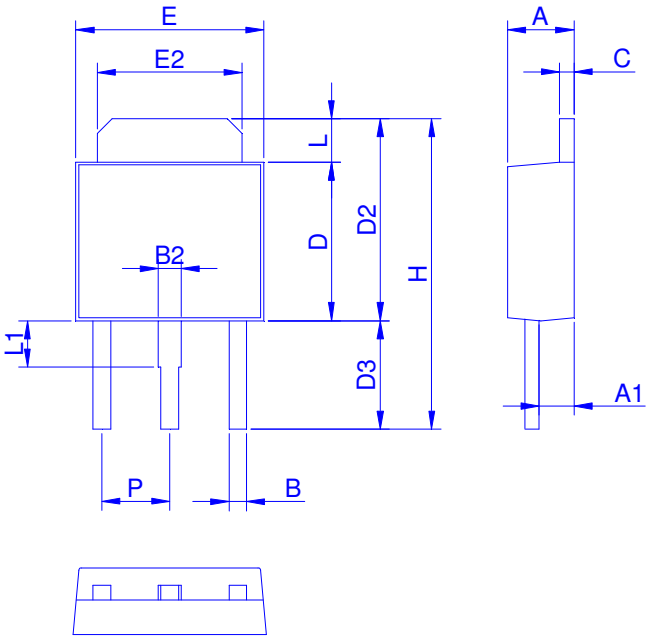
[3]Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: LB70N08E for IPAK (TO-251)



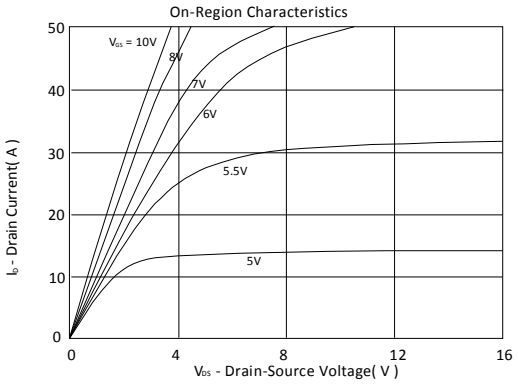
Outline Drawing

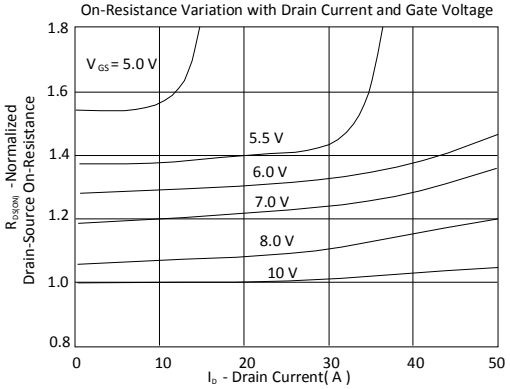


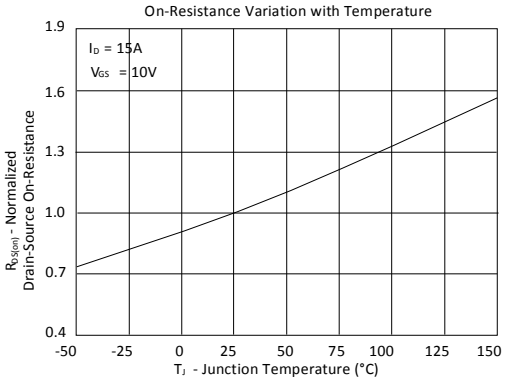
Dimension in mm

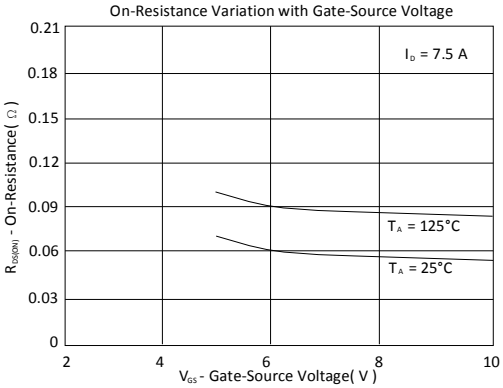
Dimension	A	A1	B	B2	C	D	D2	D3	E	E2	H	L	L1	P
Min.	2.18	0.89	0.63	0.76	0.46	5.97	6.86	3.2	6.35	4.95	10.06	0.89		
Nom.	2.29		0.76			6.10		3.3	6.60				1.05	2.29
Max.	2.39	1.14	0.85	1.05	0.61	6.22	7.49	3.4	6.73	5.46	10.89	1.27		

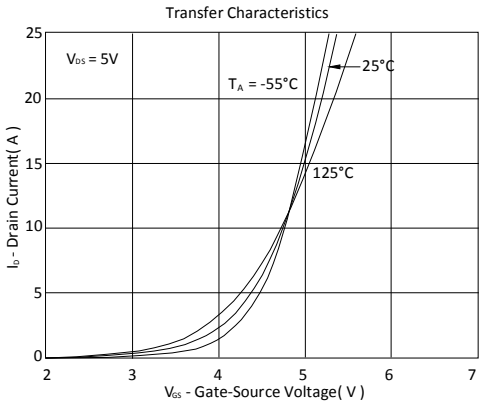
TYPICAL CHARACTERISTICS

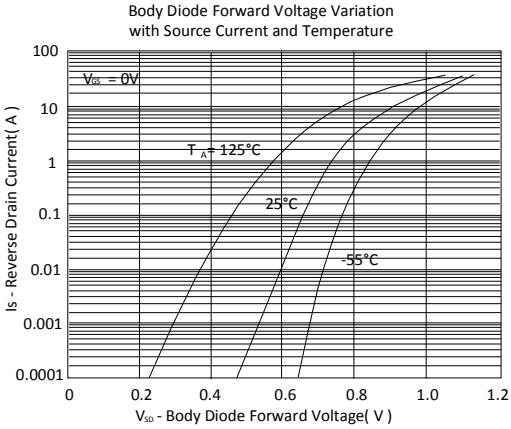


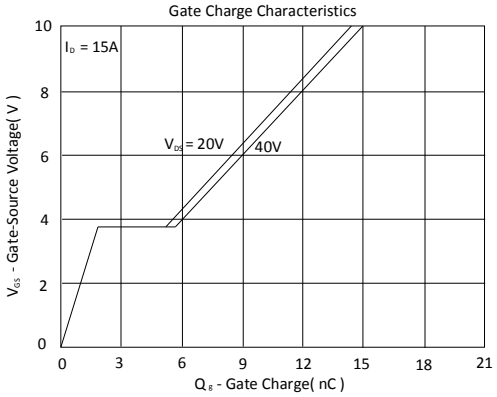


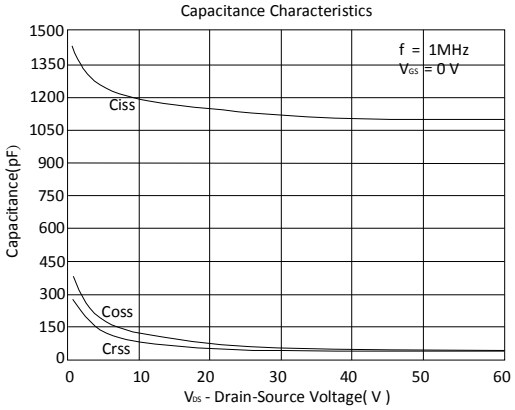


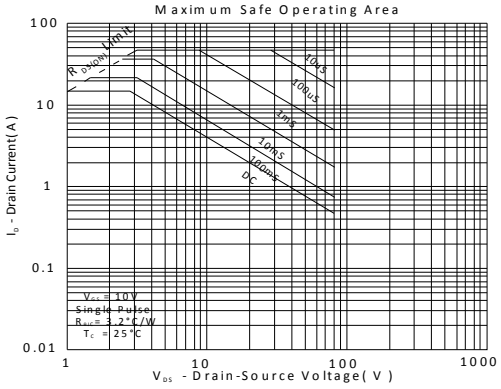


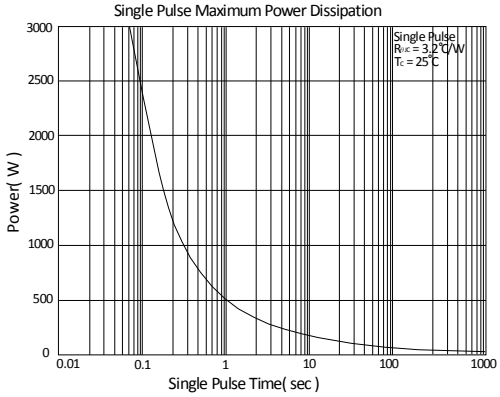


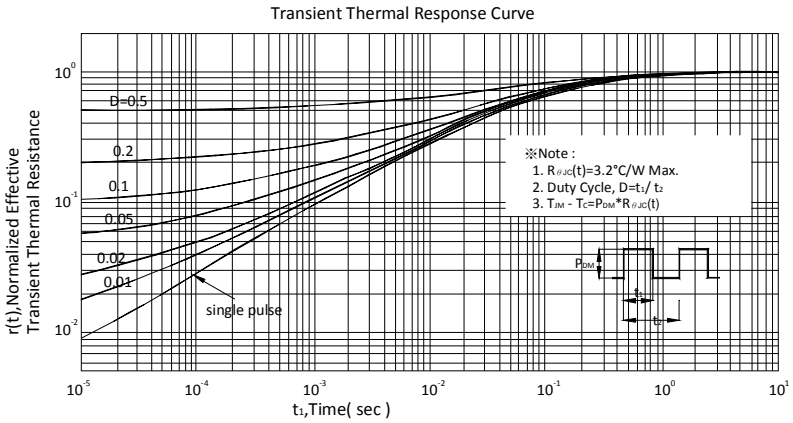



Gate Charge Characteristics
I_D = 15A
V_{DS} = 20V
40V
V_{GS} - Gate-Source Voltage(V)
Q_g - Gate Charge(nC)


Capacitance Characteristics
f = 1MHz
V_{GS} = 0 V
Ciss
Coss
Crss
Capacitance(pF)
V_{DS} - Drain-Source Voltage(V)


Maximum Safe Operating Area
$R_{DS(ON)}$ Limit
10mS
100uS
1mS
10mS
100mS
DC
V_{GS} = 10 V
Single Pulse
$R_{\theta JC}$ = 3.2°C/W
T_C = 25°C
I_D - Drain Current(A)
V_{DS} - Drain-Source Voltage(V)


Single Pulse Maximum Power Dissipation
Single Pulse
$R_{\theta JC}$ = 3.2°C/W
T_C = 25°C
Power(W)
Single Pulse Time(sec)


Transient Thermal Response Curve
D=0.5
0.2
0.1
0.05
0.02
0.01
single pulse
※Note :
1. $R_{\theta JC}$(t)=3.2°C/W Max.
2. Duty Cycle, D=t_1/ t_2
3. T_{JM} - T_C=P_{DM}*$R_{\theta JC}$(t)
P_{DM}
t_1
t_2
r(t),Normalized Effective Transient Thermal Resistance
t_1,Time(sec)