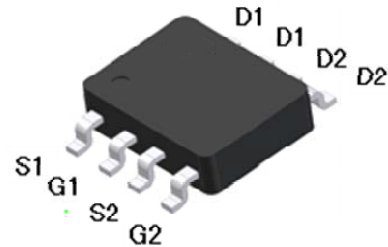
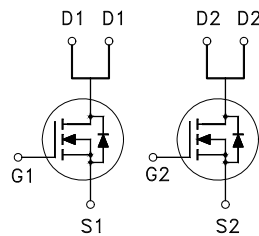


Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	60V
R _{DS(on)} (MAX.)	60mΩ
I _D	5A



UIS, R_g 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _A = 25 °C	I _D	5	A
	T _A = 100 °C		3.6	
Pulsed Drain Current ¹		I _{DM}	20	
Avalanche Current		I _{AS}	12	mJ
Avalanche Energy	L = 0.1mH, I _D =12A, R _G =25Ω	E _{AS}	7.2	
Repetitive Avalanche Energy ²	L = 0.05mH	E _{AR}	3.6	
Power Dissipation	T _A = 25 °C	P _D	2	W
	T _A = 100 °C		0.8	
Operating Junction & Storage Temperature Range		T _j , T _{stg}	-55 to 150	°C

100% UIS testing in condition of V_D=30V, L=0.1mH, V_G=10V, I_L=5A, Rated V_{DS}=60V N-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}		25	°C / W
Junction-to-Ambient ³	R _{θJA}		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

³62.5°C / W when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ($T_c = 25\text{ }^{\circ}\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT	
			MIN	TYP	MAX		
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	60			V	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.0	2.0	3.2		
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 48V, V_{GS} = 0V$			1	μA	
		$V_{DS} = 40V, V_{GS} = 0V, T_J = 125\text{ }^{\circ}C$			25		
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 5V, V_{GS} = 10V$	5			A	
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 5A$		50	60	m Ω	
		$V_{GS} = 4.5V, I_D = 4A$		70	85		
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 5A$		13		S	
DYNAMIC							
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 30V, f = 1MHz$		633		pF	
Output Capacitance	C_{oss}			67			
Reverse Transfer Capacitance	C_{rss}			44			
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = 30V, V_{GS} = 10V,$ $I_D = 5A$		13.8		nC	
Gate-Source Charge ^{1,2}	Q_{gs}			2.8			
Gate-Drain Charge ^{1,2}	Q_{gd}			4.0			
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = 30V,$ $I_D = 1A, V_{GS} = 10V, R_{GS} = 6\Omega$		10		nS	
Rise Time ^{1,2}	t_r			7.5			
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			15			
Fall Time ^{1,2}	t_f			10			
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_c = 25\text{ }^{\circ}C$)							
Continuous Current	I_S				2.3	A	
Pulsed Current ³	I_{SM}				9.2		
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			1.2	V	

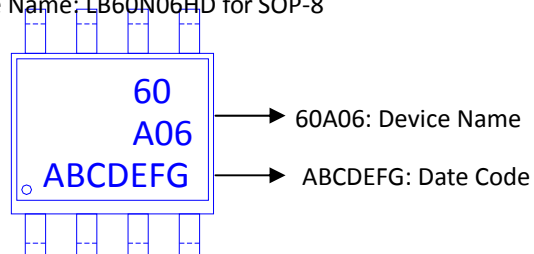
¹Pulse test : Pulse Width $\leq 300\text{ }\mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

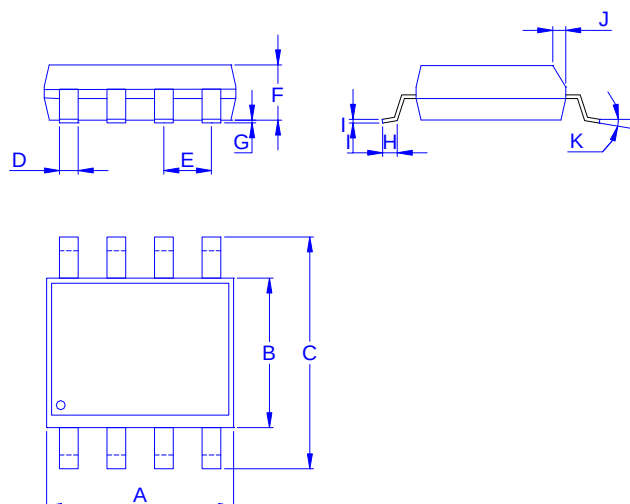
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: LB60N06HD for SOP-8



Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°

