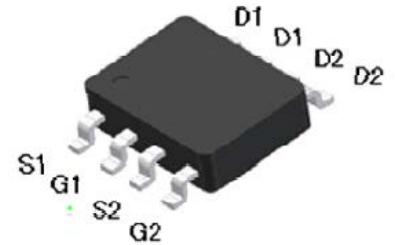
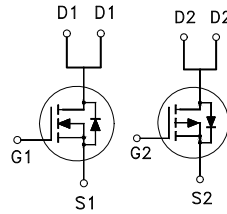


N & P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

	N-CH	P-CH
BV_{DSS}	60V	-60V
$R_{DS(on)} (MAX.)$	60m Ω	90m Ω
I_D	5A	-4A



Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
Gate-Source Voltage		V _{GS}	N-CH	P-CH	V
			±20	±20	
Continuous Drain Current	T _A = 25 °C	I _D	5	-4	A
	T _A = 100 °C		3.6	-2.8	
Pulsed Drain Current ¹		I _{DM}	20	-16	
Power Dissipation	T _A = 25 °C	P _D	2		W
	T _A = 100 °C		0.8		
Operating Junction & Storage Temperature Range		T _j , T _{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		25	$^\circ\text{C} / \text{W}$
Junction-to-Ambient ³	$R_{\theta JA}$		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³62.5 $^\circ\text{C} / \text{W}$ when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA V _{GS} = 0V, I _D = -250μA	N-CH	60		V
			P-CH	-60		
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA V _{DS} = V _{GS} , I _D = -250μA	N-CH	1.0	1.7	3.0
			P-CH	-1.0	-1.7	-3.0
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V V _{DS} = 0V, V _{GS} = ±20V	N-CH			±100
			P-CH			±100
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 48V, V _{GS} = 0V V _{DS} = -48V, V _{GS} = 0V	N-CH			1
			P-CH			-1
		V _{DS} = 40V, V _{GS} = 0V, T _J = 125 °C V _{DS} = -40V, V _{GS} = 0V, T _J = 125 °C	N-CH			25
			P-CH			-25
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 5V, V _{GS} = 10V V _{DS} = -5V, V _{GS} = -10V	N-CH	5		A
			P-CH	-4		
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 10V, I _D = 5A V _{GS} = -10V, I _D = -4A	N-CH		50	60
			P-CH		78	90
		V _{GS} = 4.5V, I _D = 4A V _{GS} = -4.5V, I _D = -2.5A	N-CH		60	85
			P-CH		100	135
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 5A V _{DS} = -5V, I _D = -4A	N-CH		13	S
			P-CH		9	
DYNAMIC						
Input Capacitance	C _{iss}	N-CH V _{GS} = 0V, V _{DS} = 30V, f = 1MHz P-CH V _{GS} = 0V, V _{DS} = -30V, f = 1MHz	N-CH		633	pF
Output Capacitance	C _{oss}		P-CH		963	
			N-CH		67	
Reverse Transfer Capacitance	C _{rss}		P-CH		76	
			N-CH		44	
			P-CH		61	

Total Gate Charge ^{1,2}	Q _g	N-CH V _{DS} = 30V, V _{GS} = 10V, I _D = 5A P-CH V _{DS} = -30V, V _{GS} = -10V, I _D = -4A	N-CH		13.8		nC
Gate-Source Charge ^{1,2}	Q _{gs}		P-CH		16.2		
Gate-Drain Charge ^{1,2}	Q _{gd}		N-CH		2.8		
			P-CH		2.0		
			N-CH		4.0		
			P-CH		3.5		
Turn-On Delay Time ^{1,2}	t _{d(on)}	N-CH V _{DS} = 30V, I _D = 1A, V _{GS} = 10V, R _{GS} = 6Ω	N-CH		10		nS
Rise Time ^{1,2}	t _r		P-CH		10		
			N-CH		7.5		
			P-CH		12		
Turn-Off Delay Time ^{1,2}	t _{d(off)}	P-CH V _{DS} = -30V, I _D = -1A, V _{GS} = -10V, R _{GS} = 6Ω	N-CH		15		
			P-CH		20		
Fall Time ^{1,2}	t _f		N-CH		10		
			P-CH		15		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _c = 25 °C)							
Continuous Current	I _S		N-CH			5	A
			P-CH			-4	
Pulsed Current ³	I _{SM}		N-CH			20	
			P-CH			-16	
Forward Voltage ¹	V _{SD}	I _F = I _S , V _{GS} = 0V	N-CH			1.3	
			P-CH			-1.3	

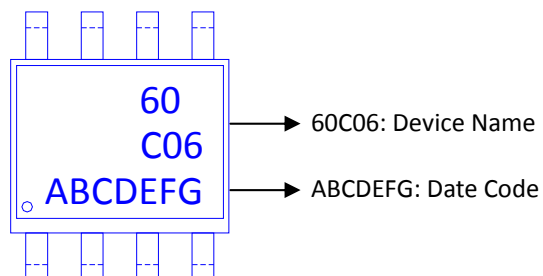
¹Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

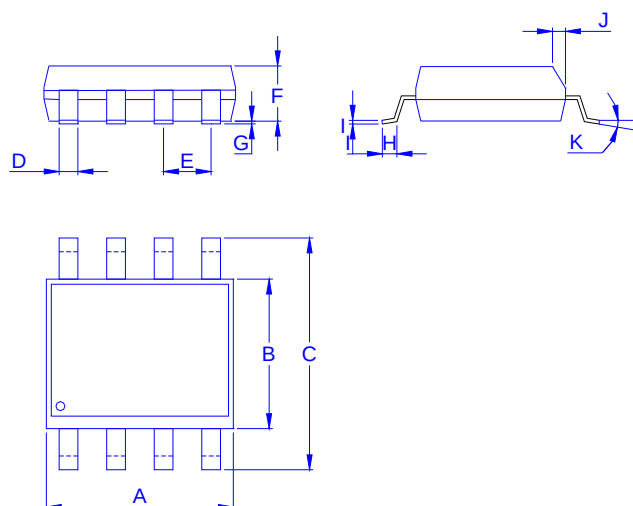
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: LB60C06H for SOP-8



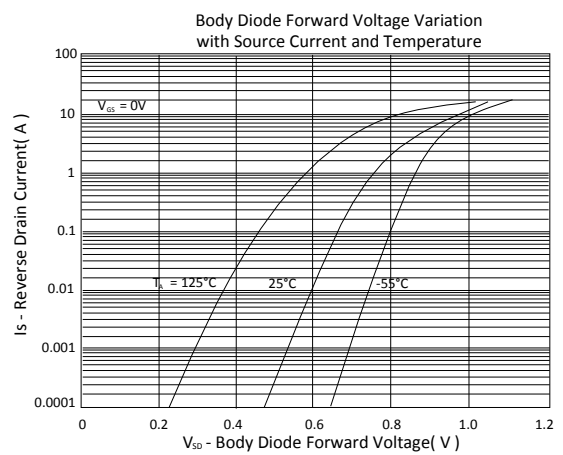
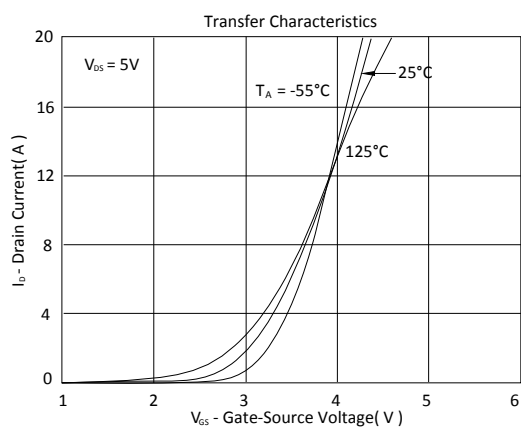
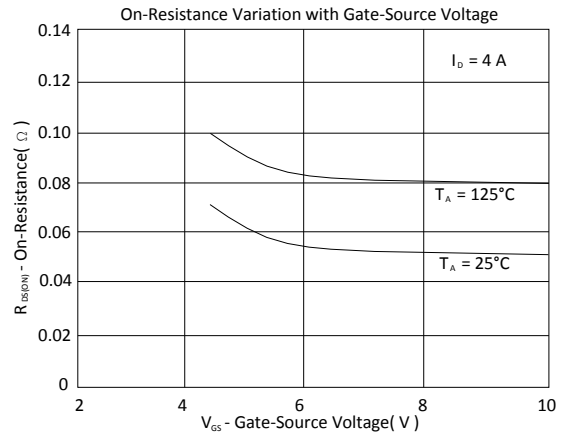
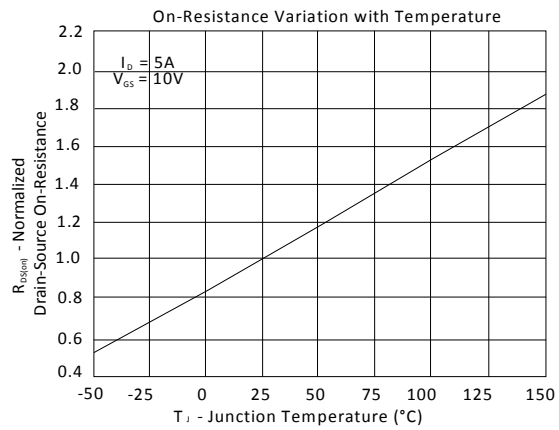
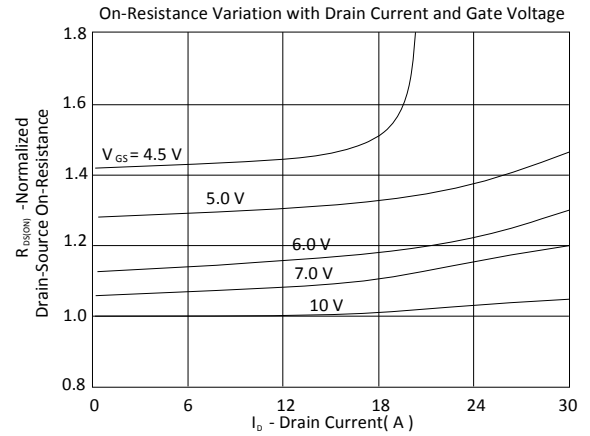
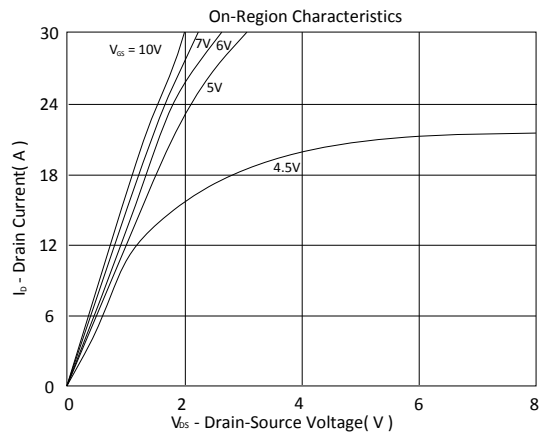
Outline Drawing

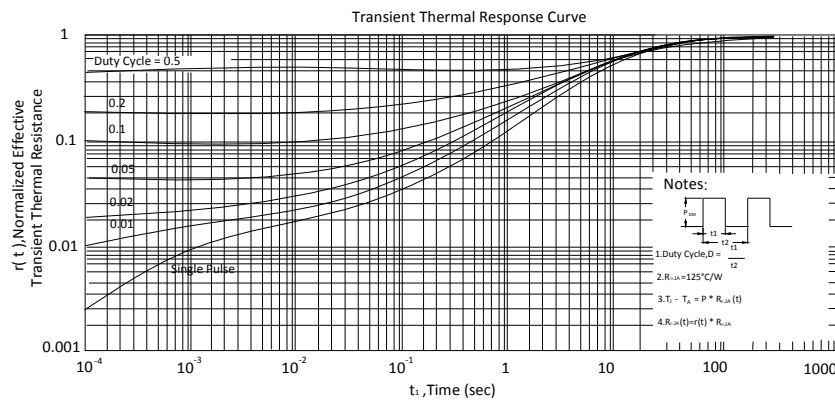
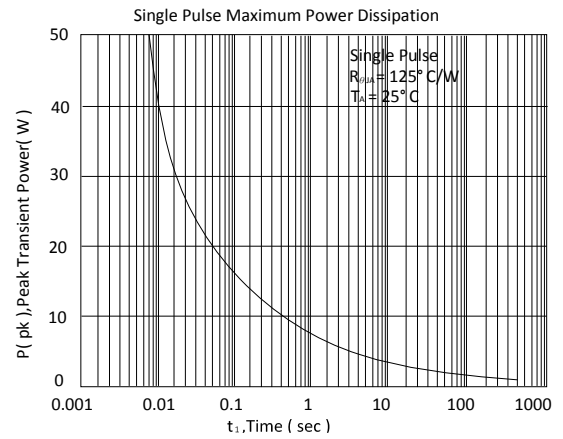
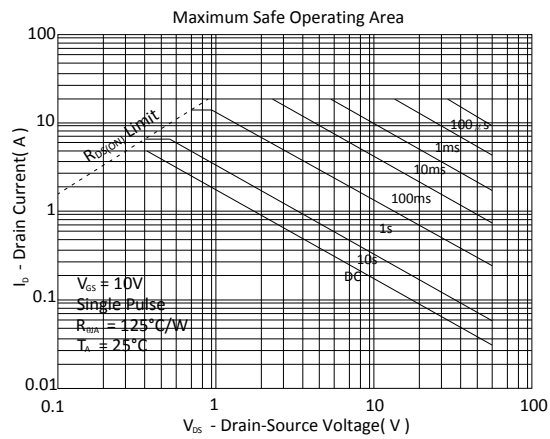
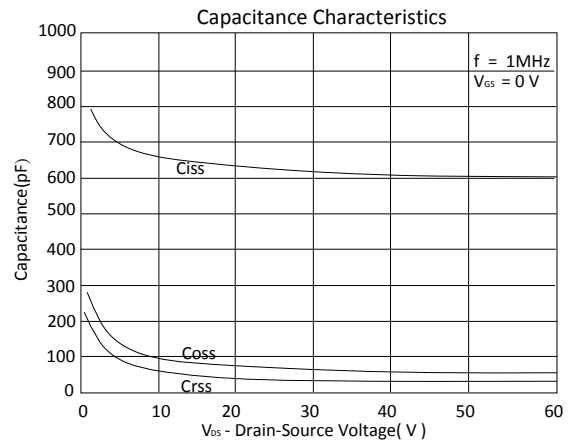
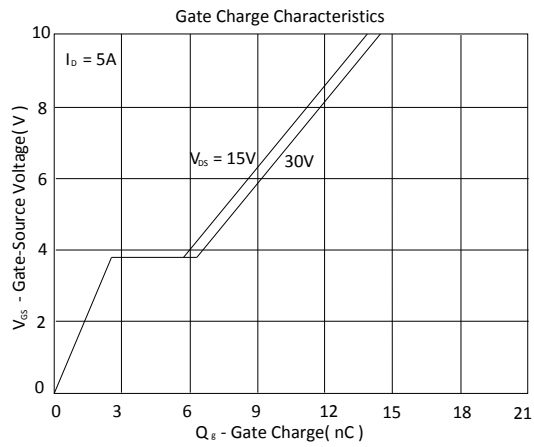


Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°

N-Channel





P-Channel

