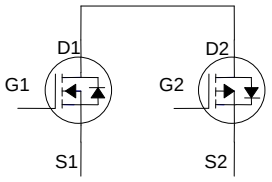
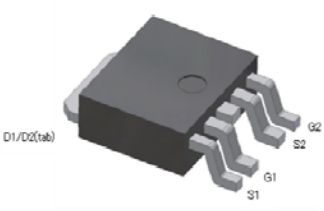
N & P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

	N-CH	P-CH
BV_{DSS}	25V	-25V
$R_{DSON\ (MAX.)}$	20mΩ	60mΩ
I_D	15A	-10A





Pb-Free Lead Plating & Halogen Free

GP
GREEN PRODUCT

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
Gate-Source Voltage		V_{GS}	N-CH	P-CH	V
			±20	±20	
Continuous Drain Current	T_C = 25 °C	I_D	15	-10	A
	T_C = 100 °C		10	-6.5	
Pulsed Drain Current[1]		I_{DM}	60	-40	
Power Dissipation	T_C = 25 °C	P_D	21		W
	T_C = 100 °C		8.3		
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		6	°C / W
Junction-to-Ambient	$R_{\theta JA}$		90	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	N-CH	25			V
		V_{GS} = 0V, I_D = -250μA	P-CH	-25			
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	N-CH	1	1.7	3	
		V_{DS} = V_{GS}, I_D = -250μA	P-CH	-0.7	-1.3	-2	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	N-CH			±100	nA
		V_{DS} = 0V, V_{GS} = ±20V	P-CH			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0V	N-CH			1	μA
		V_{DS} = -20V, V_{GS} = 0V	P-CH			-1	
		V_{DS} = 20V, V_{GS} = 0V, T_J = 125 °C	N-CH			25	
		V_{DS} = -20V, V_{GS} = 0V, T_J = 125 °C	P-CH			-25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5V, V_{GS} = 10V	N-CH	15			A
		V_{DS} = -5V, V_{GS} = -10V	P-CH	-10			
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 15A	N-CH		15.5	20	mΩ
		V_{GS} = -10V, I_D = -10A	P-CH		48	60	
		V_{GS} = 5V, I_D = 10A	N-CH		23	30	
		V_{GS} = -5V, I_D = -8A	P-CH		60	80	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 15A	N-CH		15		S
		V_{DS} = -5V, I_D = -10A	P-CH		16		
DYNAMIC							
Input Capacitance	C_{iss}	N-CH	N-CH		520		pF
		V_{GS} = 0V, V_{DS} = 15V, f = 1MHz	P-CH		520		
Output Capacitance	C_{oss}	P-CH	N-CH		88		
		V_{GS} = 0V, V_{DS} = -15V, f = 1MHz	P-CH		82		
Reverse Transfer Capacitance	C_{rss}		N-CH		62		
			P-CH		61		

Total Gate Charge[1,2]	Q_g	N-CH V_{DS} = 15V, V_{GS} = 10V, I_D = 15A P-CH V_{DS} = -15V, V_{GS} = -10V, I_D = -10A	N-CH		11.5		nC
			P-CH		8.6		
Gate-Source Charge[1,2]	Q_{gs}		N-CH		1.6		
			P-CH		1.4		
Gate-Drain Charge[1,2]	Q_{gd}		N-CH		2.8		
			P-CH		1.8		
Turn-On Delay Time[1,2]	$t_{d(on)}$	N-CH V_{DS} = 15V, I_D = 15A, V_{GS} = 10V, R_{GS} = 12.7Ω P-CH V_{DS} = -15V, I_D = -10A, V_{GS} = -10V, R_{GS} = 6Ω	N-CH		11		nS
			P-CH		5.5		
Rise Time[1,2]	t_r		N-CH		16		
			P-CH		10		
Turn-Off Delay Time[1,2]	$t_{d(off)}$		N-CH		36		
			P-CH		18		
Fall Time[1,2]	t_f		N-CH		20		
			P-CH		15		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)							
Continuous Current	I_S		N-CH			2.3	A
			P-CH			-2.3	
Pulsed Current[3]	I_{SM}		N-CH			9.2	
			P-CH			-9.2	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V	N-CH			1.3	V
			P-CH			-1.3	

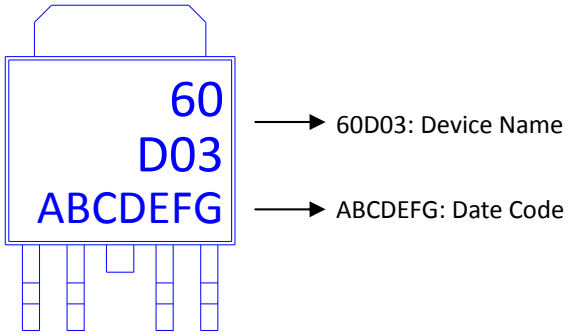
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

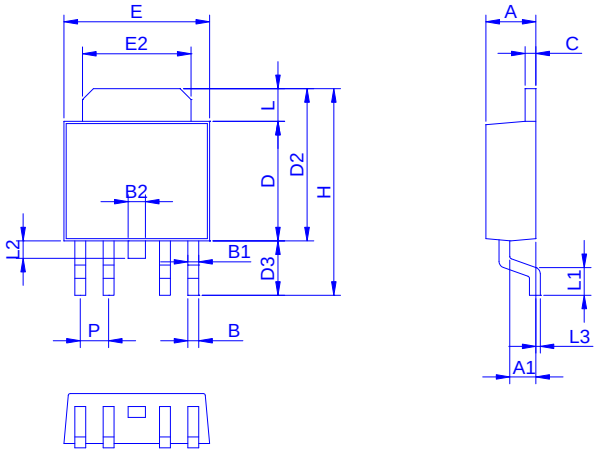
[3]Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: LB60C03D for DPAK (TO-252)

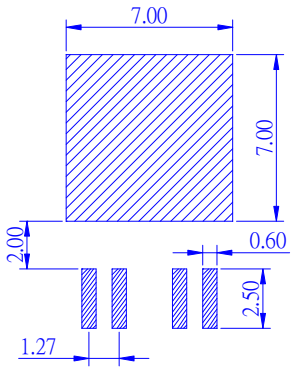


Outline Drawing

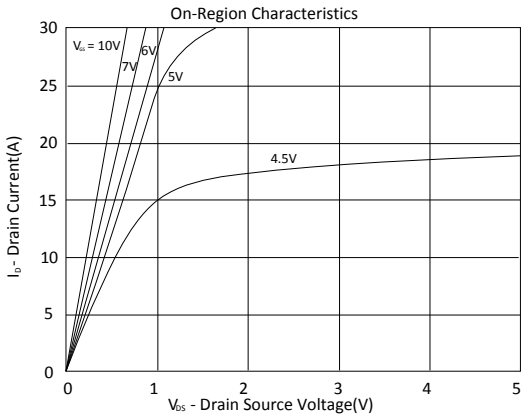


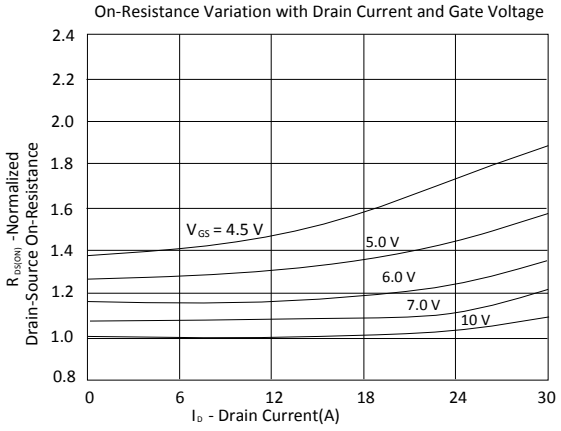
Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	1.10	0.30	0.55	0.40	0.40	5.30	6.70	2.20	6.30	4.80	9.20	1.30	0.90	0.50	0.00	1.17
Max.	2.50	1.30	0.70	0.75	0.80	0.60	5.70	7.30	3.00	6.70	5.45	10.15	1.70	1.50	1.10	0.30	1.37

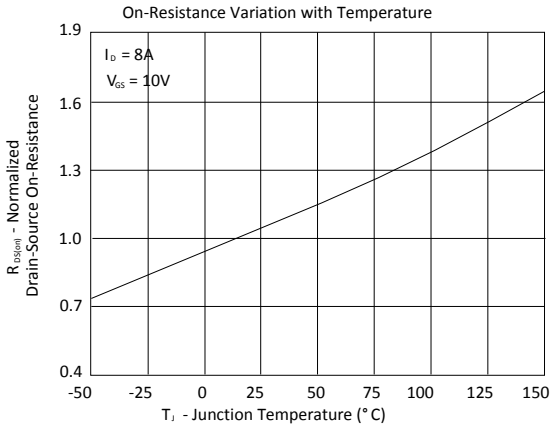
Footprint

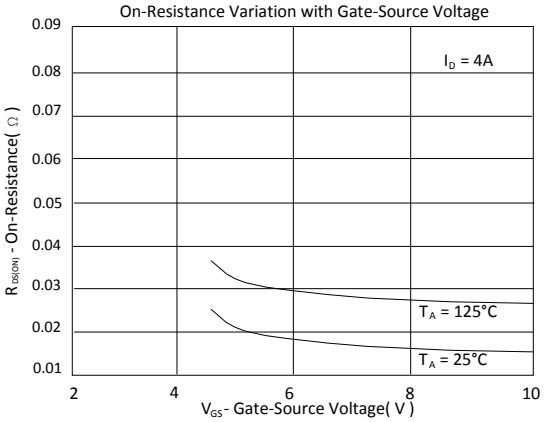


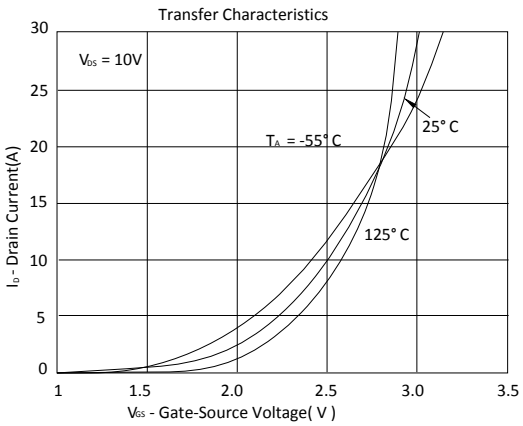
N-Channel

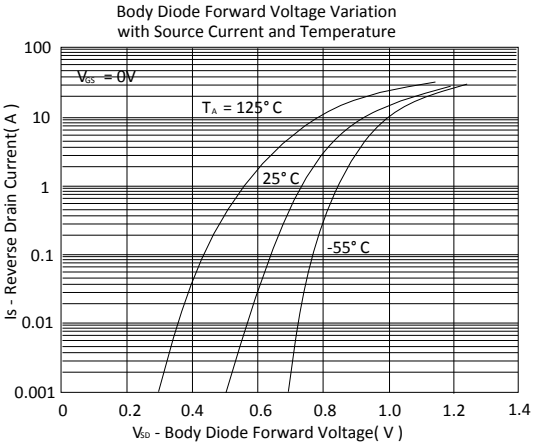

On-Region Characteristics
V_{GS} = 10V
7V
6V
5V
4.5V
I_D - Drain Current(A)
V_{DS} - Drain Source Voltage(V)


On-Resistance Variation with Drain Current and Gate Voltage
V_{GS} = 4.5 V
5.0 V
6.0 V
7.0 V
10 V
$R_{DS(ON)}$ -Normalized
Drain-Source On-Resistance
I_D - Drain Current(A)

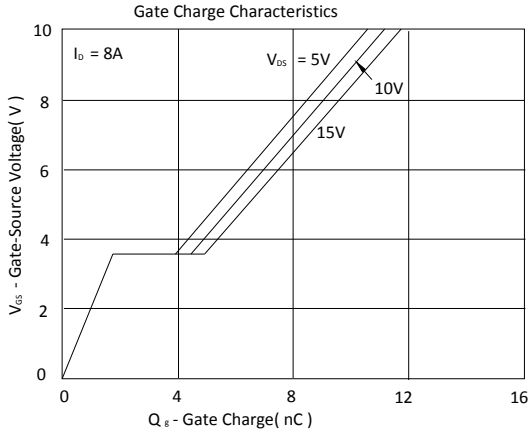

On-Resistance Variation with Temperature
I_D = 8A
V_{GS} = 10V
$R_{DS(on)}$ - Normalized
Drain-Source On-Resistance
T_J - Junction Temperature (°C)


On-Resistance Variation with Gate-Source Voltage
I_D = 4A
T_A = 125°C
T_A = 25°C
$R_{DS(ON)}$ - On-Resistance(Ω)
V_{GS}- Gate-Source Voltage(V)

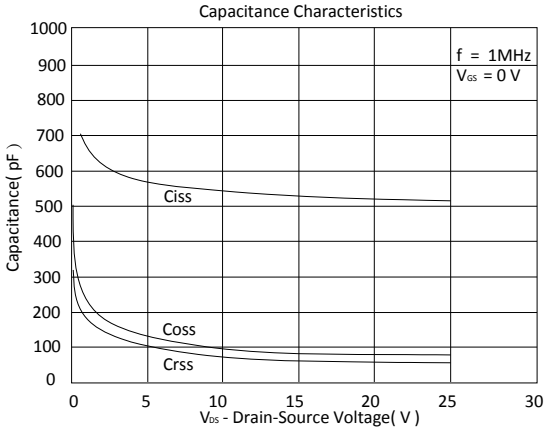

Transfer Characteristics
V_{DS} = 10V
T_A = -55° C
25° C
125° C
I_D - Drain Current(A)
V_{GS} - Gate-Source Voltage(V)


Body Diode Forward Voltage Variation
with Source Current and Temperature
V_{GS} = 0V
T_A = 125° C
25° C
-55° C
Is - Reverse Drain Current(A)
V_{SD} - Body Diode Forward Voltage(V)

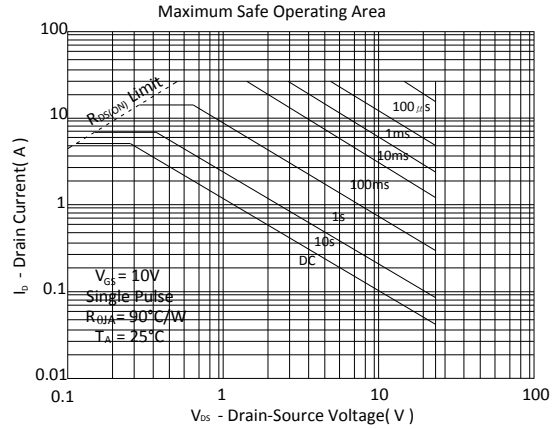
Gate Charge Characteristics



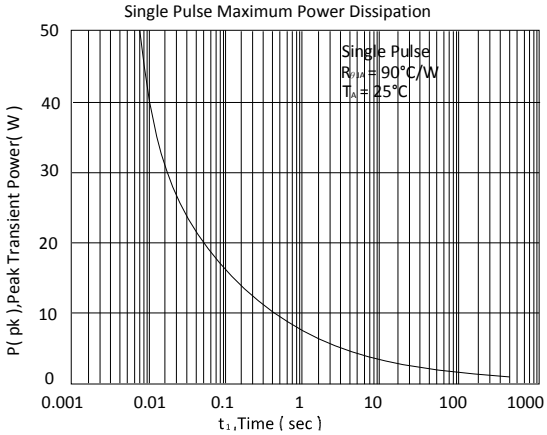
Capacitance Characteristics



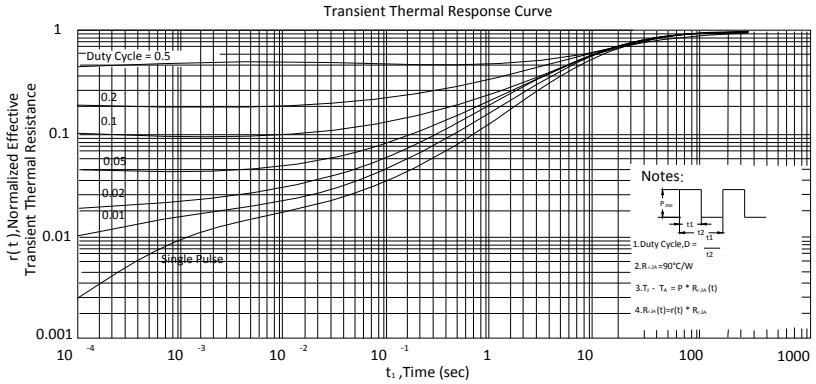
Maximum Safe Operating Area



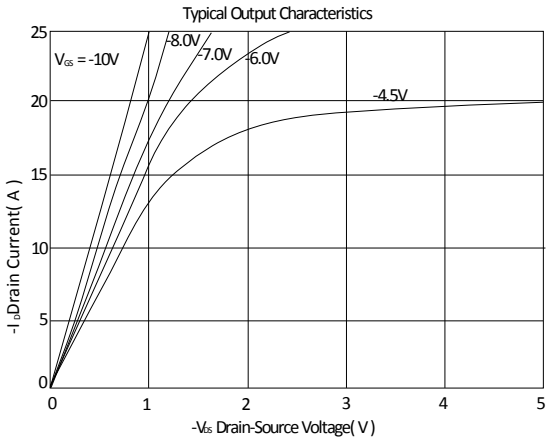
Single Pulse Maximum Power Dissipation

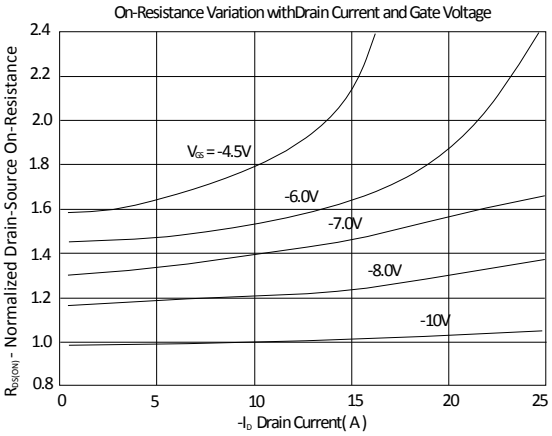


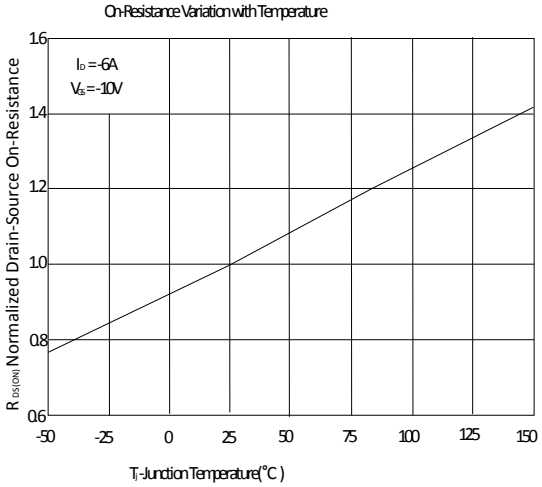
Transient Thermal Response Curve

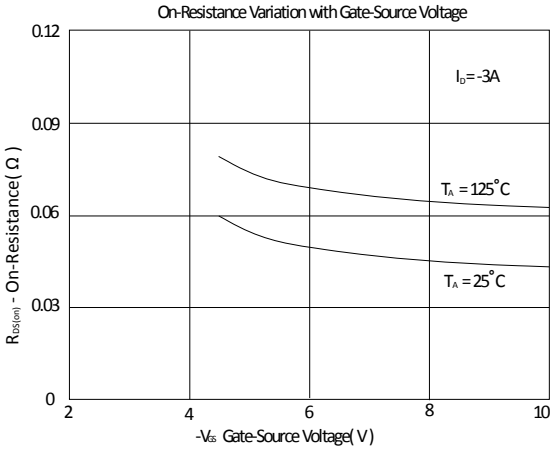


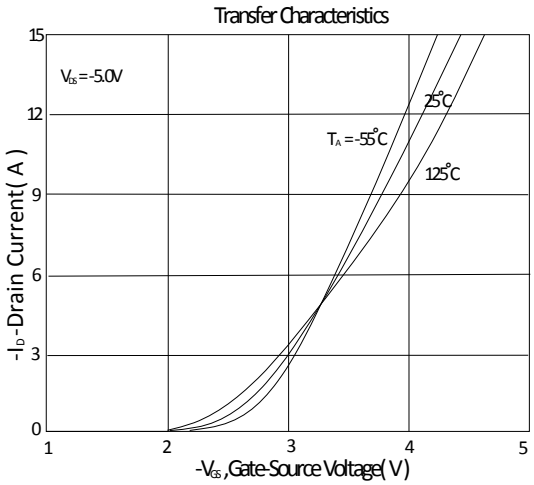
P-Channel

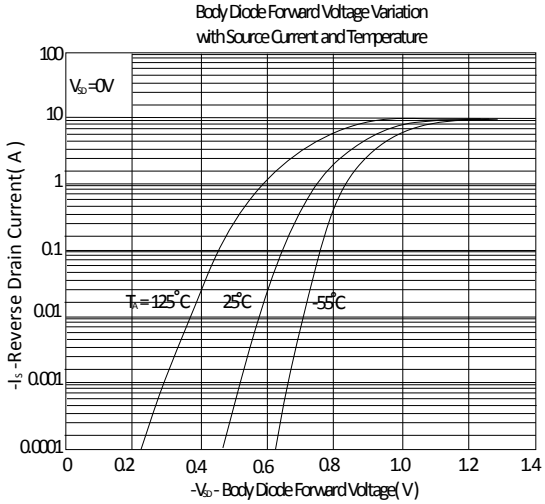

Typical Output Characteristics
V_{GS} = -10V
-8.0V
-7.0V
-6.0V
-4.5V
$-I_D$,Drain Current(A)
$-V_{DS}$ Drain-Source Voltage(V)

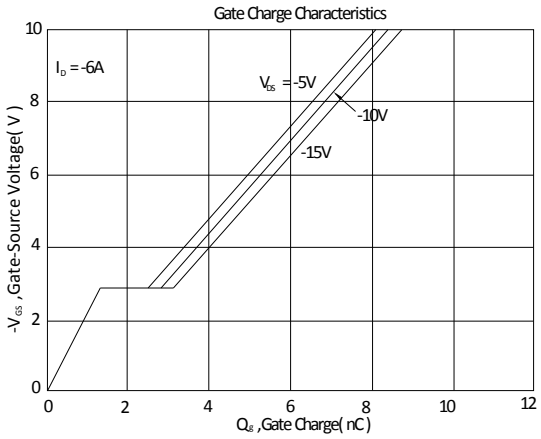

On-Resistance Variation withDrain Current and Gate Voltage
V_{GS} = -4.5V
-6.0V
-7.0V
-8.0V
-10V
$R_{DS(ON)}$ - Normalized Drain-Source On-Resistance
$-I_D$ Drain Current(A)

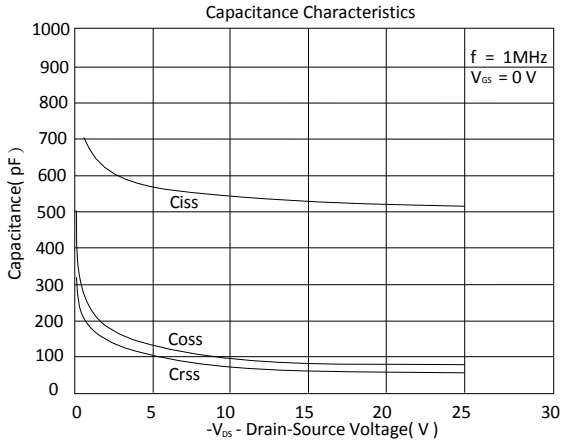

On-Resistance Variation with Temperature
I_D = -6A
V_{GS} = -10V
$R_{DS(ON)}$ Normalized Drain-Source On-Resistance
Tj-Junction Temperature(°C)

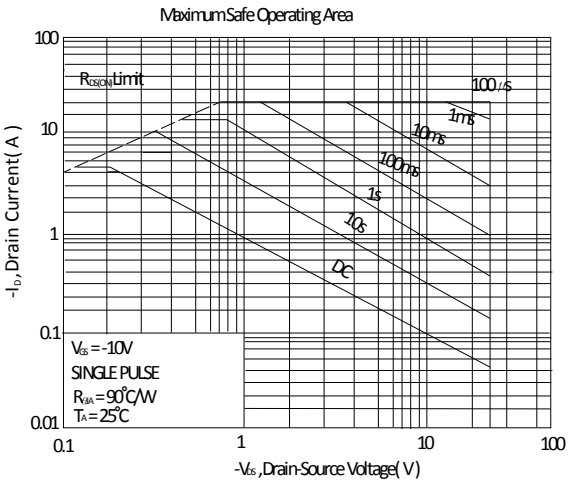

On-Resistance Variation with Gate-Source Voltage
I_D = -3A
T_A = 125°C
T_A = 25°C
$R_{DS(on)}$ - On-Resistance(Ω)
$-V_{GS}$ Gate-Source Voltage(V)

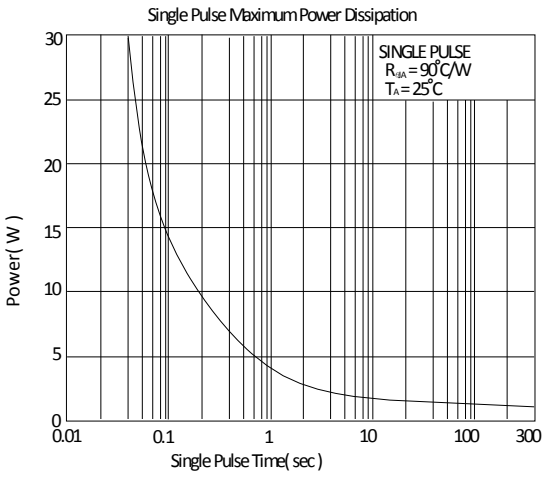

Transfer Characteristics
V_{DS} = -5.0V
25°C
T_A = -55°C
125°C
$-I_D$-Drain Current(A)
$-V_{GS}$,Gate-Source Voltage(V)

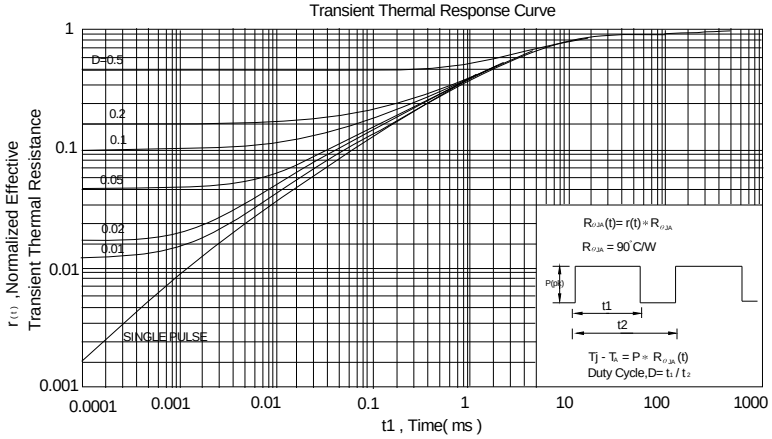

Body Diode Forward Voltage Variation
with Source Current and Temperature
V_{GS} =0V
T_A = 125°C
25°C
-55°C
$-I_S$ -Reverse Drain Current(A)
$-V_{SD}$ - Body Diode Forward Voltage(V)


Gate Charge Characteristics
I_D = -6A
V_DS = -5V
-10V
-15V
-V_GS ,Gate-Source Voltage(V)
Q_g ,Gate Charge(nC)


Capacitance Characteristics
f = 1MHz
V_GS = 0 V
Ciss
Coss
Crss
Capacitance(pF)
-V_DS - Drain-Source Voltage(V)


Maximum Safe Operating Area
R_DS(ON) Limit
100μs
1ms
10ms
100ms
1s
10s
DC
V_GS = -10V
SINGLE PULSE
R_θJA = 90°C/W
T_A = 25°C
-I_D, Drain Current(A)
-V_DS ,Drain-Source Voltage(V)


Single Pulse Maximum Power Dissipation
SINGLE PULSE
R_θJA = 90°C/W
T_A = 25°C
Power(W)
Single Pulse Time(sec)


Transient Thermal Response Curve
D=0.5
0.2
0.1
0.05
0.02
0.01
SINGLE PULSE
R_θJA(t)= r(t) * R_θJA
R_θJA = 90°C/W
P(pk)
t1
t2
Tj - T_A = P * R_θJA(t)
Duty Cycle,D= t1 / t2
r(t) ,Normalized Effective Transient Thermal Resistance
t1 , Time(ms)