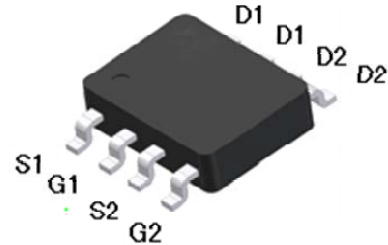
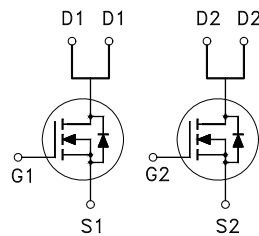


Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	30V
R _{DS(on)} (MAX.)	55mΩ
I _D	4.5A



UIS, 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _A = 25 °C	I _D	4.5	A
	T _A = 70 °C		3.3	
Pulsed Drain Current ¹		I _{DM}	18	
Avalanche Current		I _{AS}	4.5	mJ
Avalanche Energy	L = 0.1mH, I _D =4.5A, R _G =25Ω	E _{AS}	1	
Repetitive Avalanche Energy ²	L = 0.05mH	E _{AR}	0.5	
Power Dissipation	T _A = 25 °C	P _D	2	W
	T _A = 70 °C		1.3	
Operating Junction & Storage Temperature Range		T _j , T _{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}		25	°C / W
Junction-to-Ambient ³	R _{θJA}		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

³62.5°C / W when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ($T_c = 25\text{ }^{\circ}\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1	1.5	3	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 24V, V _{GS} = 0V			1	μA
		V _{DS} = 20V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	4.5			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 10V, I _D = 4.5A		45	55	mΩ
		V _{GS} = 4.5V, I _D = 3A		72	90	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 4.5A		5		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		319		pF
Output Capacitance	C _{oss}			66		
Reverse Transfer Capacitance	C _{rss}			53		
Total Gate Charge ^{1,2}	Q _g	V _{DS} = 15V, V _{GS} = 10V, I _D = 4.5A		6		nC
Gate-Source Charge ^{1,2}	Q _{gs}			0.8		
Gate-Drain Charge ^{1,2}	Q _{gd}			1.8		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{DS} = 15V, I _D = 1A, V _{GS} = 10V, R _{GS} = 6Ω		8		nS
Rise Time ^{1,2}	t _r			2.5		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			20		
Fall Time ^{1,2}	t _f			5		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _c = 25 °C)						
Continuous Current	I _S				2.1	A
Pulsed Current ³	I _{SM}				8.4	
Forward Voltage ¹	V _{SD}	I _F = I _S , V _{GS} = 0V			1.2	V
Reverse Recovery Time	t _{rr}	I _F = I _S , dI _F /dt = 100A / μS		40		nS
Peak Reverse Recovery Current	I _{RM(REC)}			20		A
Reverse Recovery Charge	Q _{rr}			1.5		nC

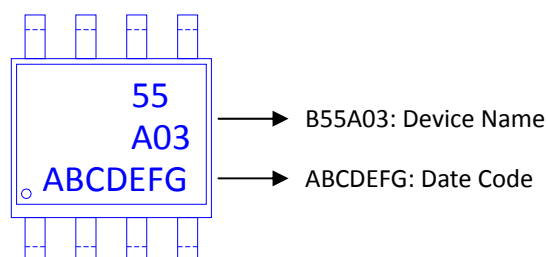
¹Pulse test : Pulse Width $\leq 300\mu$ sec, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

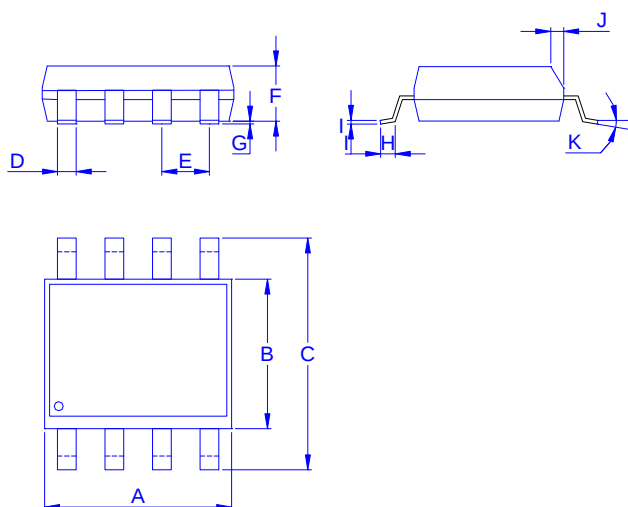
³Pulse width limited by maximum junction

temperature. **Ordering & Marking Information:**

Device Name: LB55N03HD for SOP-8



Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
in.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°

