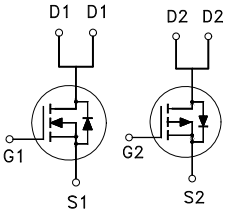
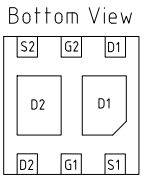
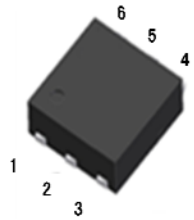
N & P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

	N-CH	P-CH
BV_{DSS}	20V	-20V
$R_{DSON\ (MAX.)}$	45mΩ	100mΩ
I_D	4.8A	-3.4A







Pb-Free Lead Plating & Halogen Free

GREEN PRODUCT

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
Gate-Source Voltage		V_{GS}	N-CH	P-CH	V
			±12	±12	
Continuous Drain Current	T_A = 25 °C	I_D	4.8	-3.4	A
	T_A = 70 °C		3.8	-2.7	
Pulsed Drain Current[1]		I_{DM}	19.2	-13.6	
Power Dissipation	T_A = 25 °C	P_D	1.9		W
	T_A = 70 °C		1.2		
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		15	°C / W
Junction-to-Ambient[3]	$R_{\theta JA}$		65	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

[3]65°C / W when mounted on a 1 in^2 pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	N-CH	20			V
		V_{GS} = 0V, I_D = -250μA	P-CH	-20			
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	N-CH	0.4	0.75	1.2	
		V_{DS} = V_{GS}, I_D = -250μA	P-CH	-0.3	-0.75	-1.2	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±12V	N-CH			±100	nA
		V_{DS} = 0V, V_{GS} = ±12V	P-CH			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16V, V_{GS} = 0V	N-CH			1	μA
		V_{DS} = -16V, V_{GS} = 0V	P-CH			-1	
		V_{DS} = 16V, V_{GS} = 0V, T_J = 125 °C	N-CH			10	
		V_{DS} = -16V, V_{GS} = 0V, T_J = 125 °C	P-CH			-10	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5V, V_{GS} = 4.5V	N-CH	4.8			A
		V_{DS} = -5V, V_{GS} = -4.5V	P-CH	-3.4			
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 4.5V, I_D = 3.5A	N-CH		36	45	mΩ
		V_{GS} = -4.5V, I_D = -3A	P-CH		83	100	
		V_{GS} = 2.5V, I_D = 2A	N-CH		43	60	
		V_{GS} = -2.5V, I_D = -2A	P-CH		110	135	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 3.5A	N-CH		5		S
		V_{DS} = -5V, I_D = -3A	P-CH		4.5		
DYNAMIC							
Input Capacitance	C_{iss}	N-CH V_{GS} = 0V, V_{DS} = 15V, f = 1MHz P-CH V_{GS} = 0V, V_{DS} = -15V, f = 1MHz	N-CH		355		pF
			P-CH		420		
Output Capacitance	C_{oss}		N-CH		56		
			P-CH		56		
Reverse Transfer Capacitance	C_{rss}		N-CH		40		
			P-CH		42		

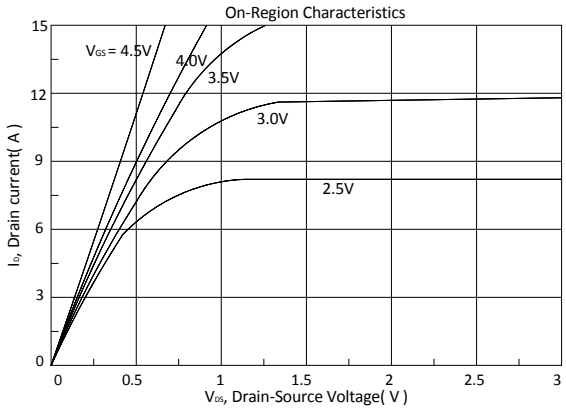
Total Gate Charge[1,2]	Q_g	N-CH V_{DS} = 10V, V_{GS} = 4.5V, I_D = 5A P-CH V_{DS} = -10V, V_{GS} = -4.5V, I_D = -3A	N-CH		4.6		nC
			P-CH		5.4		
Gate-Source Charge[1,2]	Q_{gs}		N-CH		0.66		
			P-CH		0.75		
Gate-Drain Charge[1,2]	Q_{gd}		N-CH		1.5		
			P-CH		1.3		
Turn-On Delay Time[1,2]	$t_{d(on)}$	N-CH V_{DS} = 10V, I_D = 1A, V_{GS} = 4.5V, R_{GS} = 6Ω P-CH V_{DS} = -10V, I_D = -1A, V_{GS} = -4.5V, R_{GS} = 6Ω	N-CH		8		nS
			P-CH		10		
Rise Time[1,2]	t_r		N-CH		10		
			P-CH		20		
Turn-Off Delay Time[1,2]	$t_{d(off)}$		N-CH		20		
			P-CH		15		
Fall Time[1,2]	t_f		N-CH		15		
			P-CH		12		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)							
Continuous Current	I_S		N-CH			2	A
			P-CH			-2	
Pulsed Current[3]	I_{SM}		N-CH			8	
			P-CH			-8	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V	N-CH			1.3	V
			P-CH			-1.3	

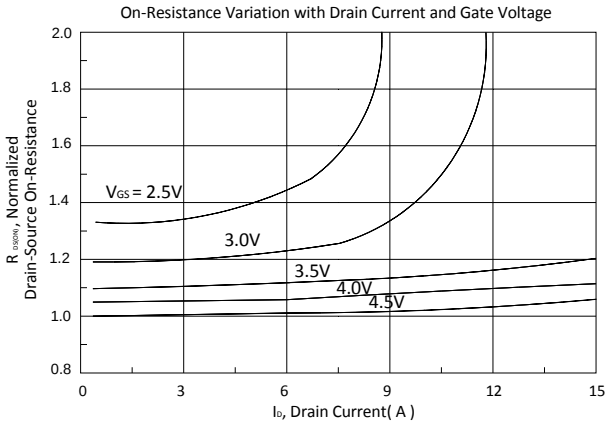
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

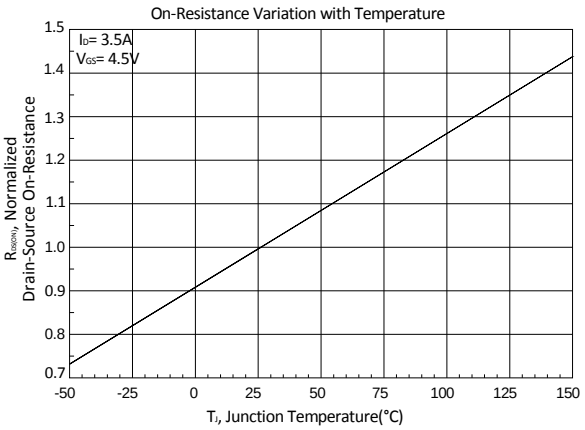
[2]Independent of operating temperature.

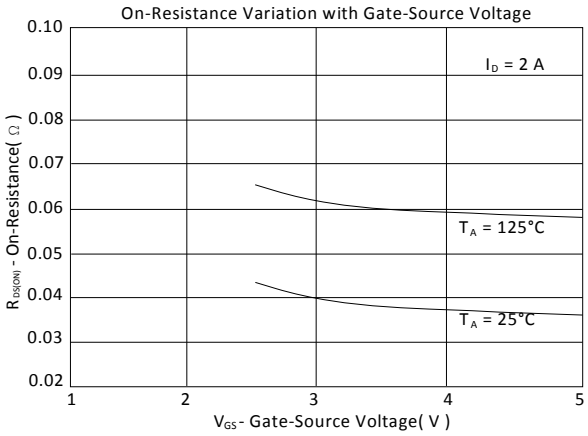
[3]Pulse width limited by maximum junction temperature.

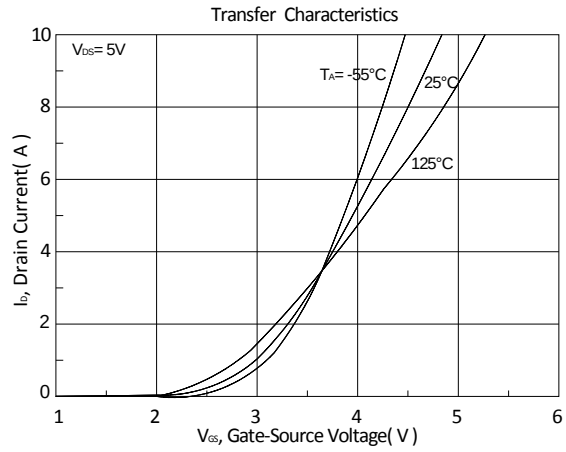
N-Channel

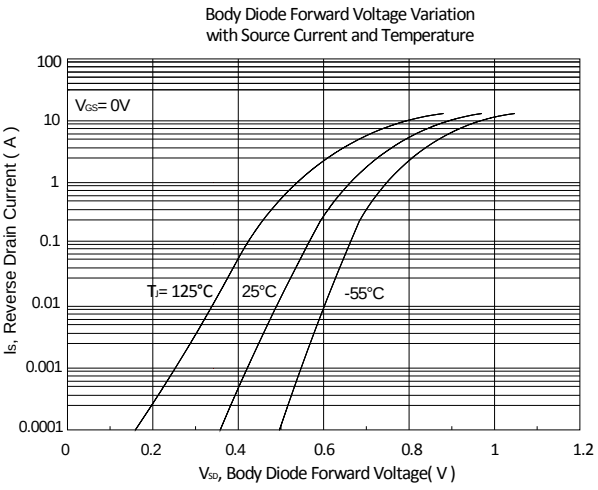

On-Region Characteristics
VGS= 4.5V
4.0V
3.5V
3.0V
2.5V
ID, Drain current(A)
VDS, Drain-Source Voltage(V)


On-Resistance Variation with Drain Current and Gate Voltage
VGS= 2.5V
3.0V
3.5V
4.0V
4.5V
RDS(ON), Normalized
Drain-Source On-Resistance
ID, Drain Current(A)

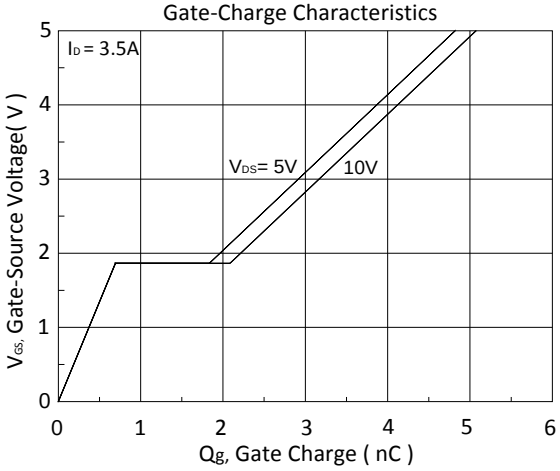

On-Resistance Variation with Temperature
ID= 3.5A
VGS= 4.5V
RDS(ON), Normalized
Drain-Source On-Resistance
TJ, Junction Temperature(°C)


On-Resistance Variation with Gate-Source Voltage
ID = 2 A
TA = 125°C
TA = 25°C
RDS(ON) - On-Resistance(Ω)
VGS - Gate-Source Voltage(V)

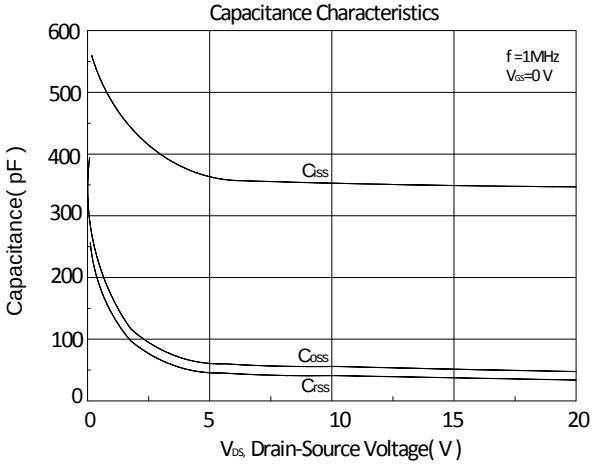

Transfer Characteristics
VDS= 5V
TA= -55°C
25°C
125°C
ID, Drain Current(A)
VGS, Gate-Source Voltage(V)


Body Diode Forward Voltage Variation
with Source Current and Temperature
VGS= 0V
TJ= 125°C
25°C
-55°C
IS, Reverse Drain Current (A)
VSD, Body Diode Forward Voltage(V)

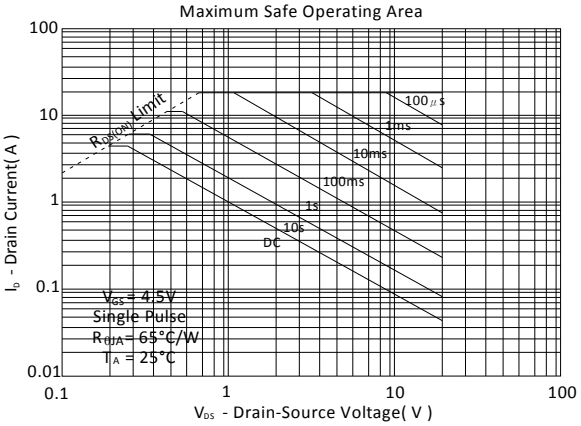
Gate-Charge Characteristics



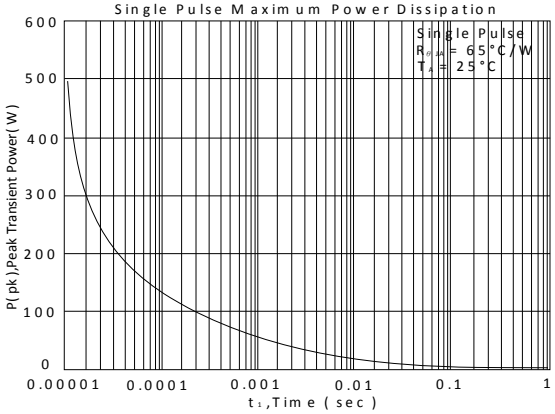
Capacitance Characteristics



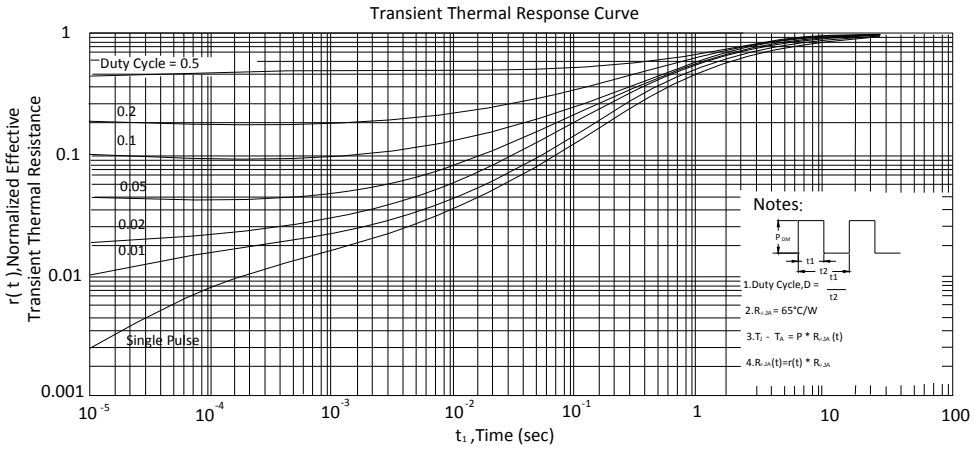
Maximum Safe Operating Area



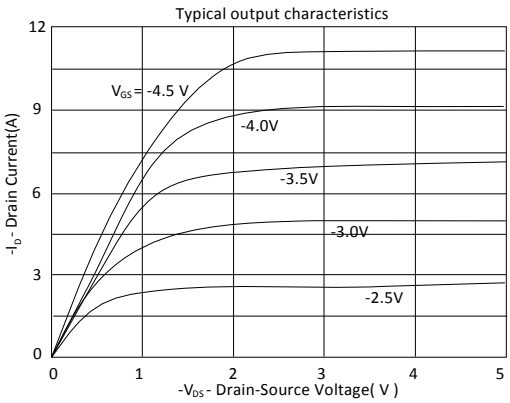
Single Pulse Maximum Power Dissipation

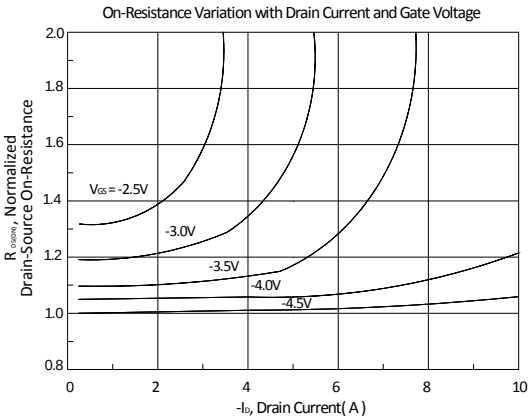


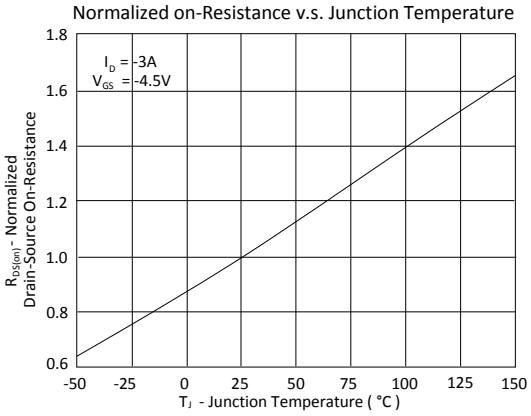
Transient Thermal Response Curve

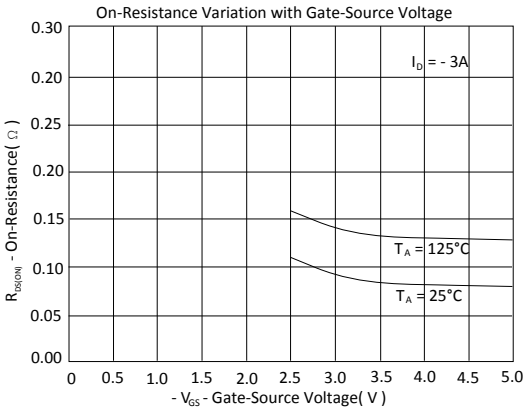


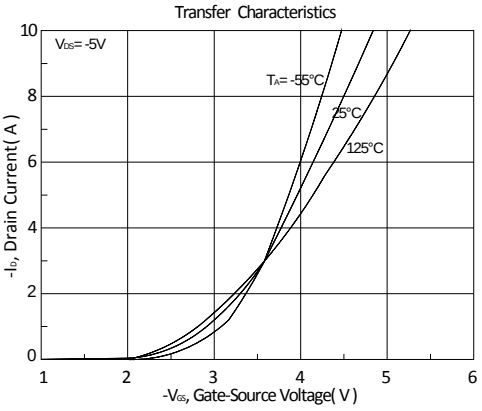
P-Channel

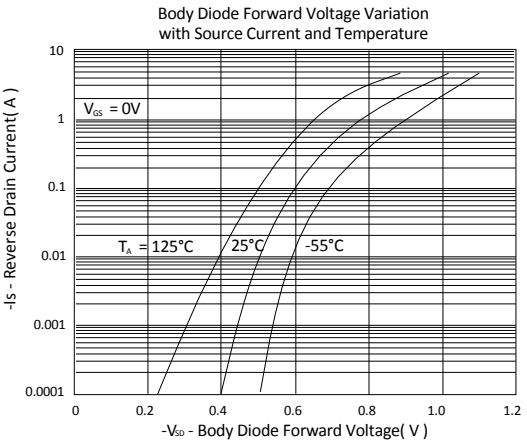

Typical output characteristics
V_{GS} = -4.5 V
-4.0V
-3.5V
-3.0V
-2.5V
$-I_D$ - Drain Current(A)
$-V_{DS}$ - Drain-Source Voltage(V)

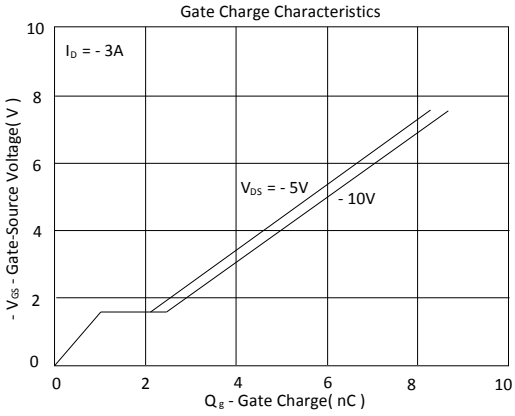

On-Resistance Variation with Drain Current and Gate Voltage
V_{GS} = -2.5V
-3.0V
-3.5V
-4.0V
-4.5V
$R_{DS(ON)}$, Normalized Drain-Source On-Resistance
$-I_D$, Drain Current(A)

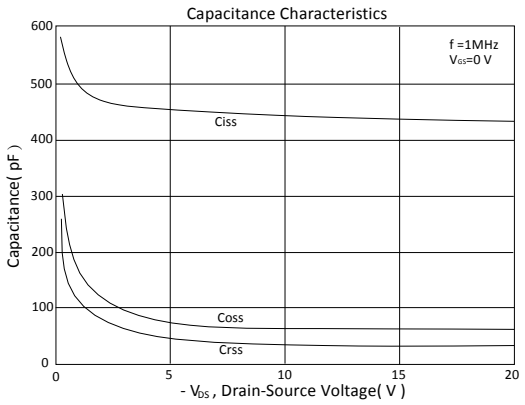

Normalized on-Resistance v.s. Junction Temperature
I_D = -3A
V_{GS} = -4.5V
$R_{DS(on)}$ - Normalized Drain-Source On-Resistance
T_J - Junction Temperature (°C)

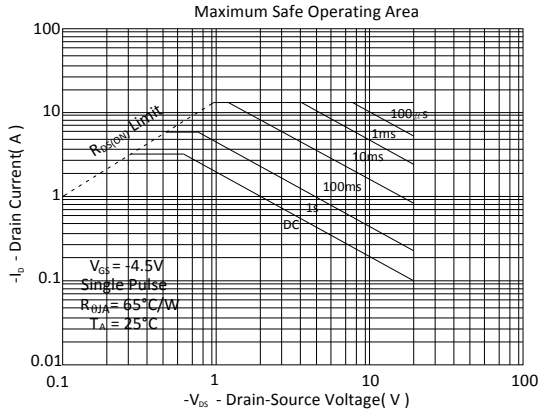

On-Resistance Variation with Gate-Source Voltage
I_D = - 3A
T_A = 125°C
T_A = 25°C
$R_{DS(ON)}$ - On-Resistance(Ω)
- V_{GS} - Gate-Source Voltage(V)

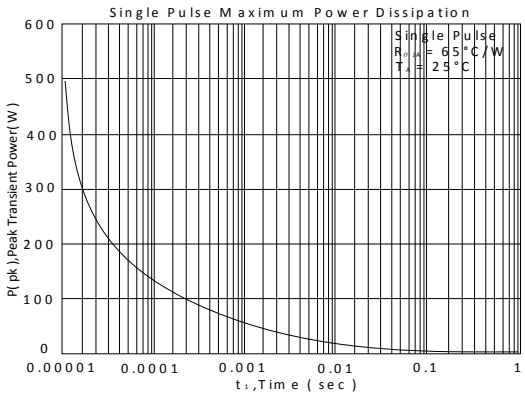

Transfer Characteristics
V_{DS}= -5V
T_A= -55°C
25°C
125°C
$-I_D$, Drain Current(A)
$-V_{GS}$, Gate-Source Voltage(V)

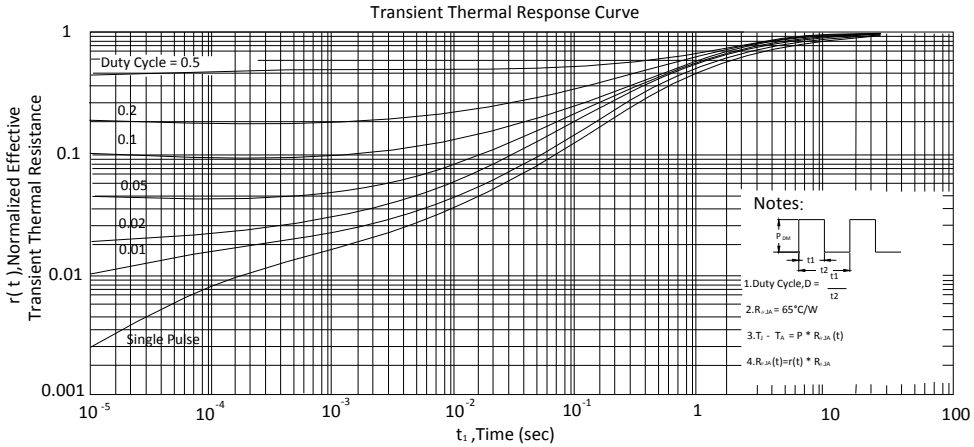

Body Diode Forward Voltage Variation with Source Current and Temperature
V_{GS} = 0V
T_A = 125°C
25°C
-55°C
-Is - Reverse Drain Current(A)
$-V_{SD}$ - Body Diode Forward Voltage(V)


Gate Charge Characteristics
I_D = - 3A
V_DS = - 5V
- 10V
- V_GS - Gate-Source Voltage(V)
Q_g - Gate Charge(nC)


Capacitance Characteristics
f =1MHz
V_GS=0 V
Ciss
Coss
Crss
Capacitance(pF)
- V_DS , Drain-Source Voltage(V)

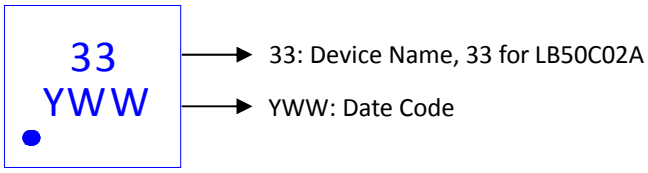

Maximum Safe Operating Area
R_DS(ON) Limit
100μs
1ms
10ms
100ms
1s
DC
V_GS = -4.5V
Single Pulse
R_θJA= 65°C/W
T_A = 25°C
-I_D - Drain Current(A)
-V_DS - Drain-Source Voltage(V)


Single Pulse Maximum Power Dissipation
Single Pulse
R_θJA = 65°C/W
T_A = 25°C
P(pk),Peak Transient Power(W)
t1 ,Time (sec)

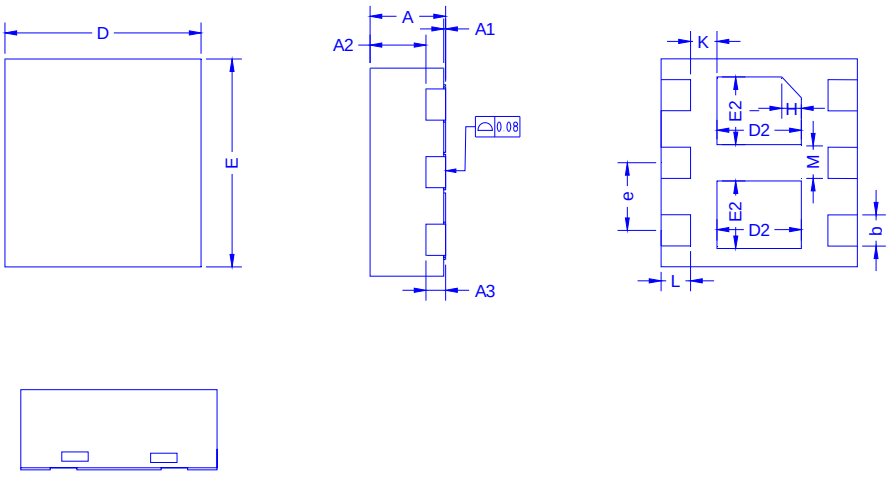

Transient Thermal Response Curve
Duty Cycle = 0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
Notes:
1.Duty Cycle,D =
2.R_θJA= 65°C/W
3.T_J - T_A = P * R_θJA (t)
4.R_θJA(t)=r(t) * R_θJA
r(t),Normalized Effective Transient Thermal Resistance
t1 ,Time (sec)

Ordering & Marking Information:

Device Name: LB50C02A for EDFN 2 x 2



Outline Drawing



Dimension in mm

Dimension	A	A1	A2	A3	b	D	E	D2	E2	e	H	K	L	M
Min.	0.70	0.00	0.50	0.20 REF	0.25	1.90	1.90	0.76	0.55	0.55	0.20 REF	0.17	0.25	0.25
Max.	0.80	0.05	0.60		0.35	2.10	2.10	0.96	0.75	0.75		0.37	0.35	0.45

Recommended minimum pads