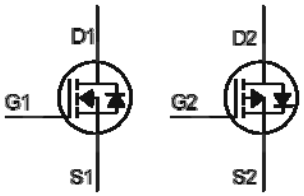
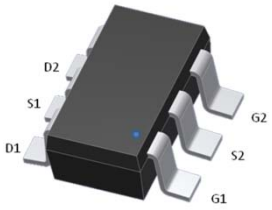
N & P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

	N-CH	P-CH
BV_{DSS}	20V	-20V
$R_{DSON\ (MAX.)}$	30.5mΩ	100mΩ
I_D	5A	-3.2A





Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
Gate-Source Voltage		V_{GS}	N-CH	P-CH	V
			±12	±12	
Continuous Drain Current	T_A = 25 °C	I_D	5	-3.2	A
	T_A = 100 °C		3.5	-2.5	
Pulsed Drain Current[1]		I_{DM}	20	-12.8	
Power Dissipation	T_A = 25 °C	P_D	1.25		W
	T_A = 70 °C		0.8		
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Ambient	$R_{\theta JA}$		100	°C / W

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS			UNIT
				MIN	TYP	MAX	
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	N-CH	20			V
		V_{GS} = 0V, I_D = -250μA	P-CH	-20			
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	N-CH	0.4	0.75	1.2	
		V_{DS} = V_{GS}, I_D = -250μA	P-CH	-0.4	-0.75	-1.2	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±12V	N-CH			±100	nA
		V_{DS} = 0V, V_{GS} = ±12V	P-CH			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16V, V_{GS} = 0V	N-CH			1	μA
		V_{DS} = -16V, V_{GS} = 0V	P-CH			-1	
		V_{DS} = 16V, V_{GS} = 0V, T_J = 125 °C	N-CH			10	
		V_{DS} = -16V, V_{GS} = 0V, T_J = 125 °C	P-CH			-10	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5V, V_{GS} = 4.5V	N-CH	5			A
		V_{DS} = -5V, V_{GS} = -4.5V	P-CH	-3.2			
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 4.5V, I_D = 5A	N-CH		26	30.5	mΩ
		V_{GS} = -4.5V, I_D = -3A	P-CH		85	100	
		V_{GS} = 2.5V, I_D = 3A	N-CH		40	50	
		V_{GS} = -2.5V, I_D = -1A	P-CH		120	150	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 5A	N-CH		7		S
		V_{DS} = -5V, I_D = -3A	P-CH		4.5		
DYNAMIC							
Input Capacitance	C_{iss}	N-CH	N-CH		280		pF
		V_{GS} = 0V, V_{DS} = 15V, f = 1MHz	P-CH		382		
Output Capacitance	C_{oss}	P-CH	N-CH		47		
		V_{GS} = 0V, V_{DS} = -15V, f = 1MHz	P-CH		70		
Reverse Transfer Capacitance	C_{rss}		N-CH		38		
			P-CH		60		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz	N-CH		2.0		Ω
			P-CH		5.0		

Total Gate Charge[1,2]	Q_g	N-CH V_{DS} = 10V, V_{GS} = 4.5V, I_D = 5A P-CH V_{DS} = -10V, V_{GS} = -4.5V, I_D = -3A	N-CH		6.2		nC
			P-CH		7.2		
Gate-Source Charge[1,2]	Q_{gs}		N-CH		0.9		
			P-CH		1.2		
Gate-Drain Charge[1,2]	Q_{gd}		N-CH		2.1		
			P-CH		2.3		
Turn-On Delay Time[1,2]	$t_{d(on)}$	N-CH V_{DS} = 10V, I_D = 1A, V_{GS} = 4.5V, R_{GS} = 6Ω P-CH V_{DS} = -10V, I_D = -1A, V_{GS} = -4.5V, R_{GS} = 6Ω	N-CH		5		nS
			P-CH		5		
Rise Time[1,2]	t_r		N-CH		10		
			P-CH		12		
Turn-Off Delay Time[1,2]	$t_{d(off)}$		N-CH		20		
			P-CH		23		
Fall Time[1,2]	t_f		N-CH		8		
			P-CH		10		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)							
Continuous Current	I_S		N-CH			2	A
			P-CH			-2	
Pulsed Current[3]	I_{SM}		N-CH			8	
			P-CH			-8	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V	N-CH			1.3	V
			P-CH			-1.3	

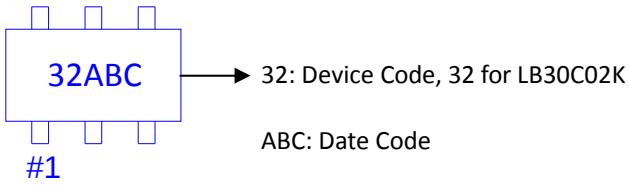
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

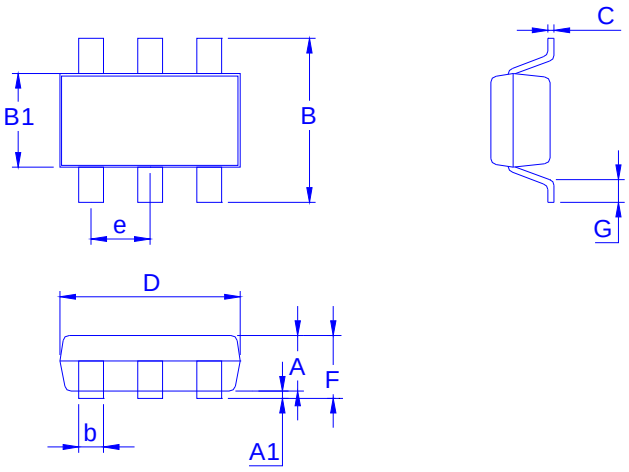
[3]Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: LB30C02K for TSOP-6



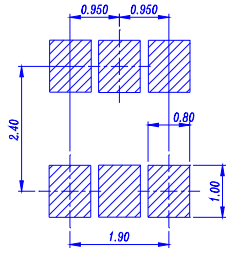
Outline Drawing



Dimension in mm

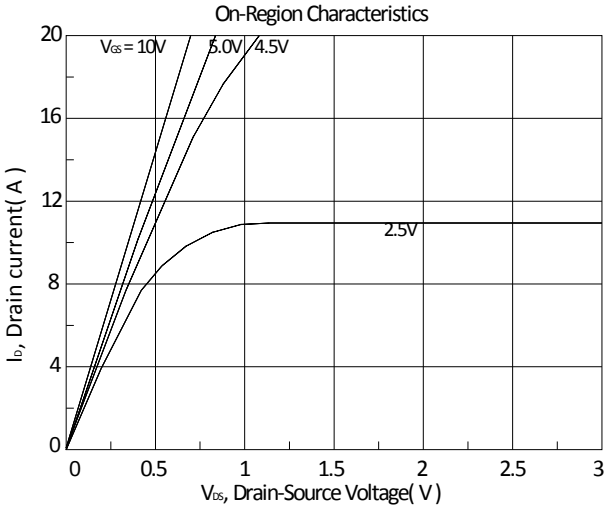
Dimension	A	A1	B	B1	b	C	D	e	F	G
Min.	0.85	0	2.50	1.50	0.30	0.08	2.70		0.85	0.20
Typ.	0.95		2.80	1.60	0.40		2.90	0.95		
Max.	1.25	0.15	3.10	1.70	0.50	0.20	3.10		1.40	0.60

Footprint

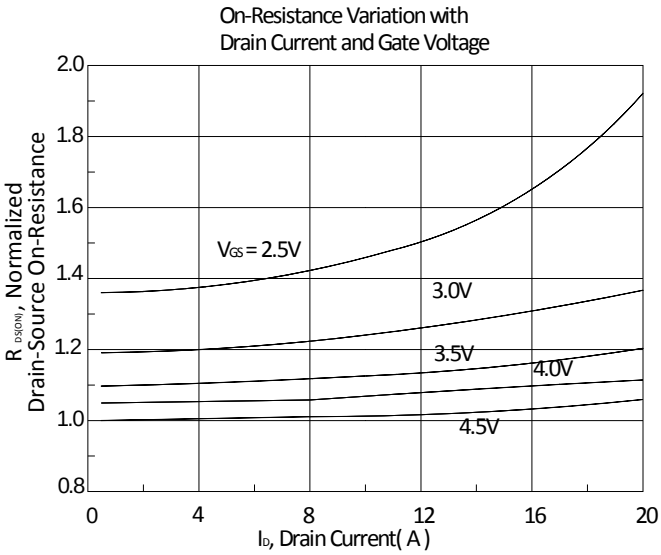


N-Channel

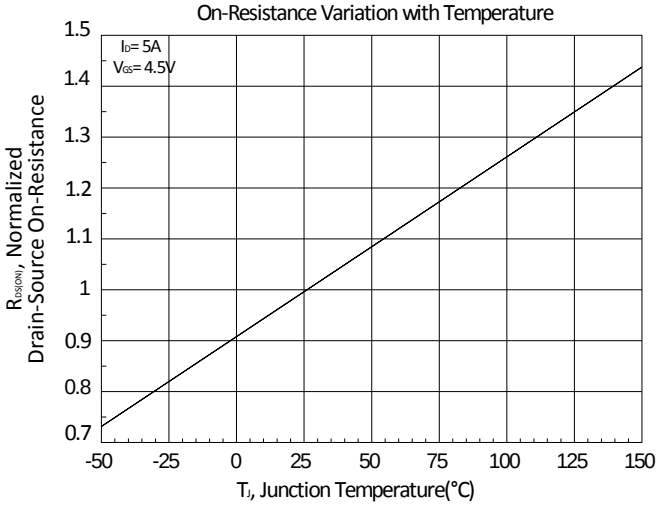
On-Region Characteristics



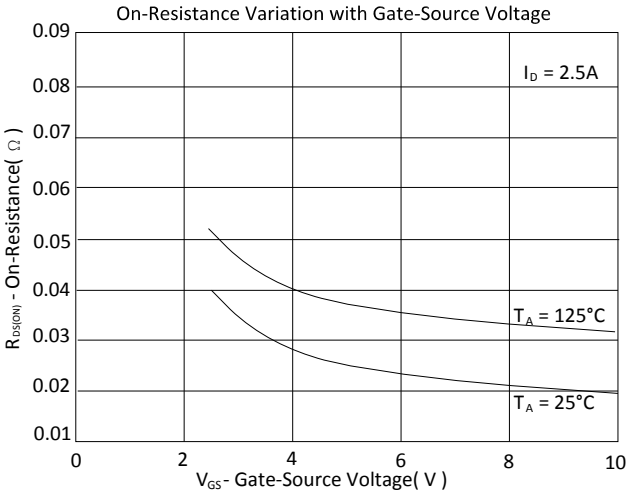
On-Resistance Variation with Drain Current and Gate Voltage



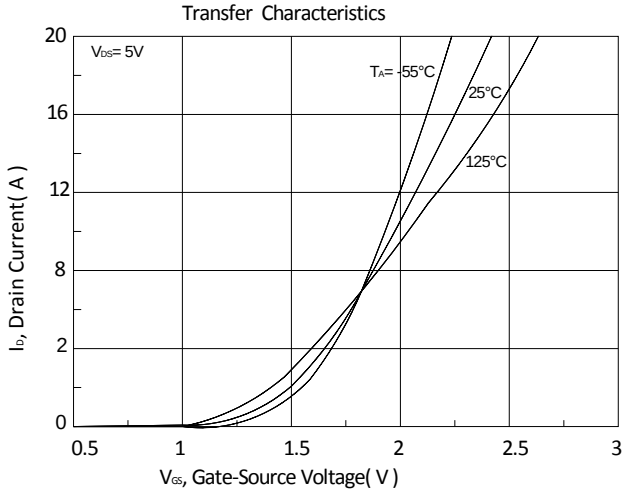
On-Resistance Variation with Temperature



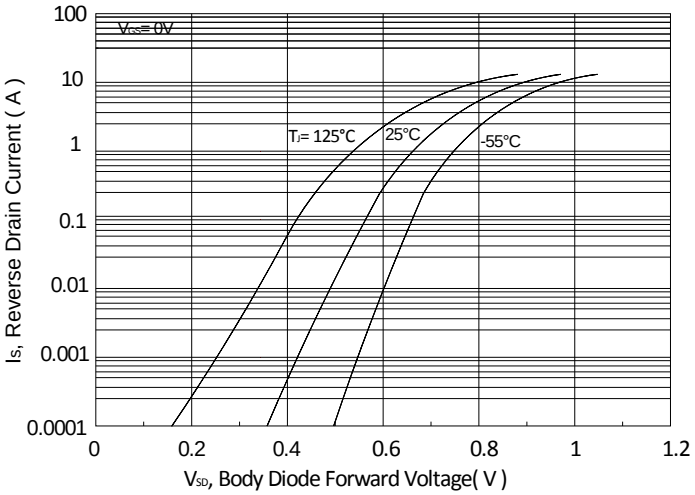
On-Resistance Variation with Gate-Source Voltage



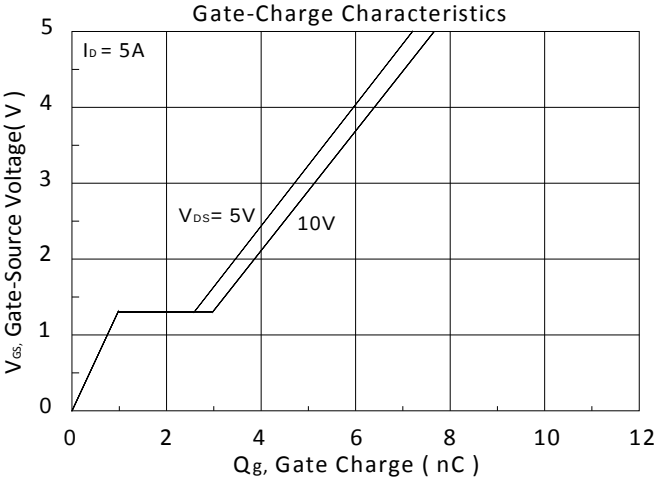
Transfer Characteristics



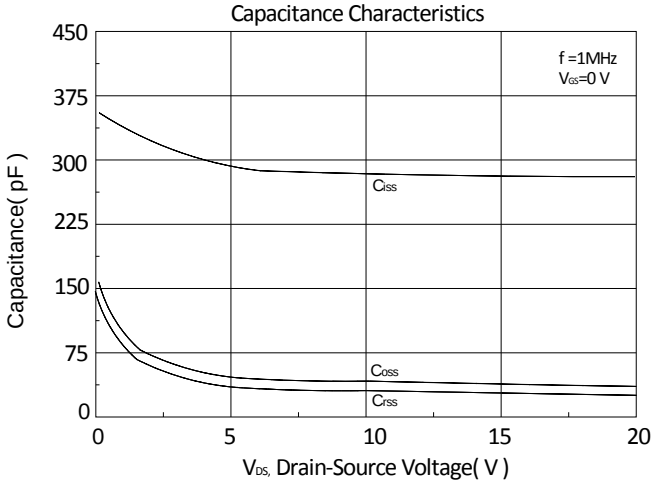
Body Diode Forward Voltage Variation with Source Current and Temperature



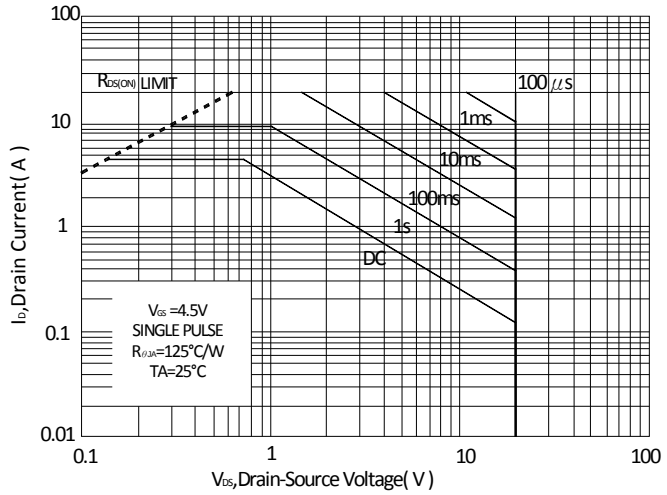
Gate-Charge Characteristics



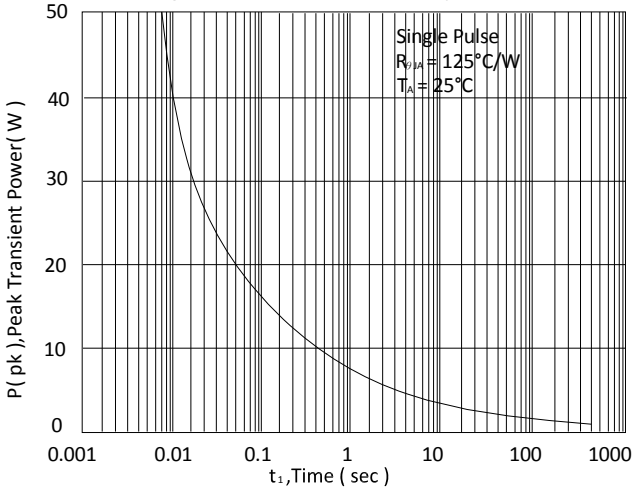
Capacitance Characteristics



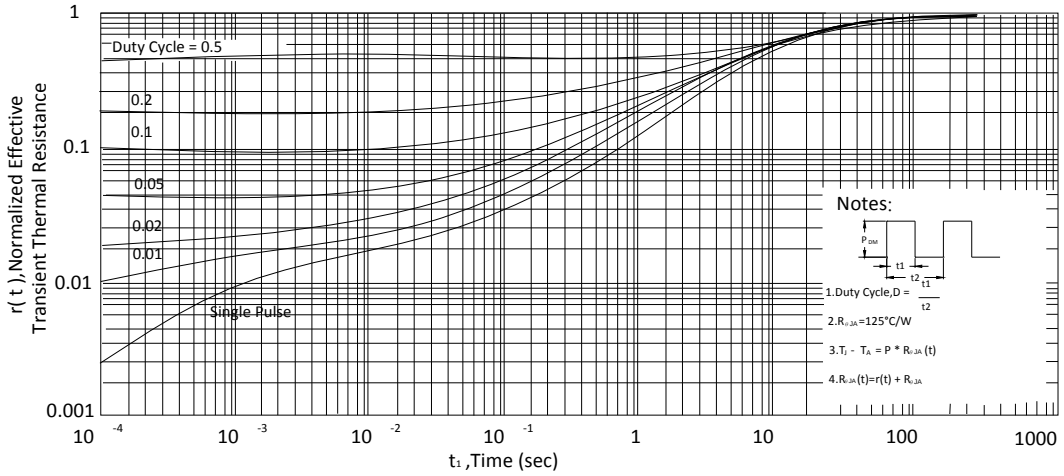
Maximum Safe Operating Area



Single Pulse Maximum Power Dissipation

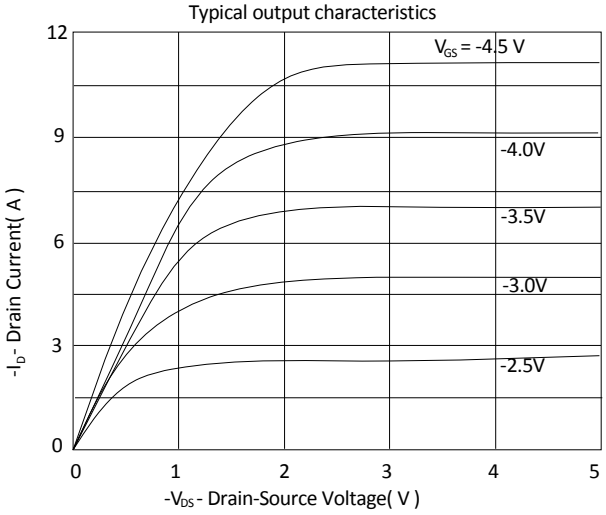


Transient Thermal Response Curve

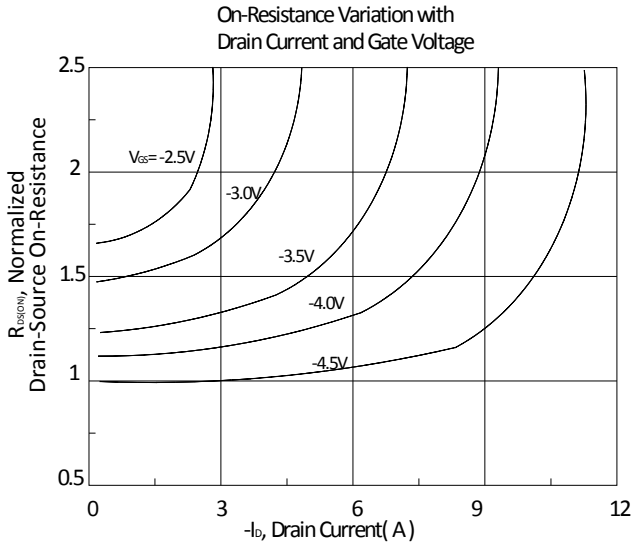


P-Channel

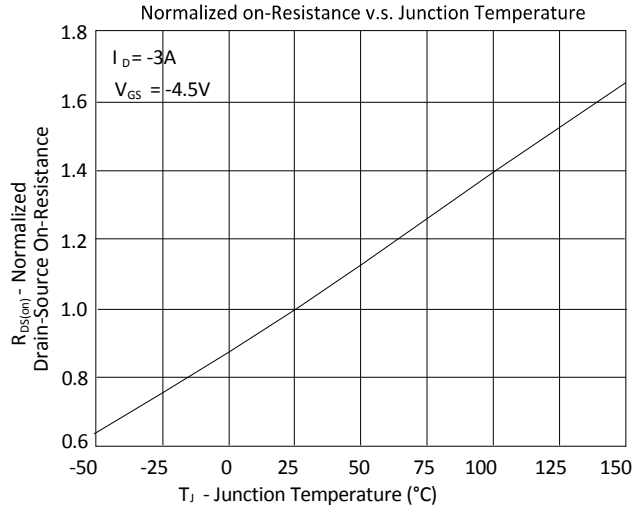
Typical output characteristics



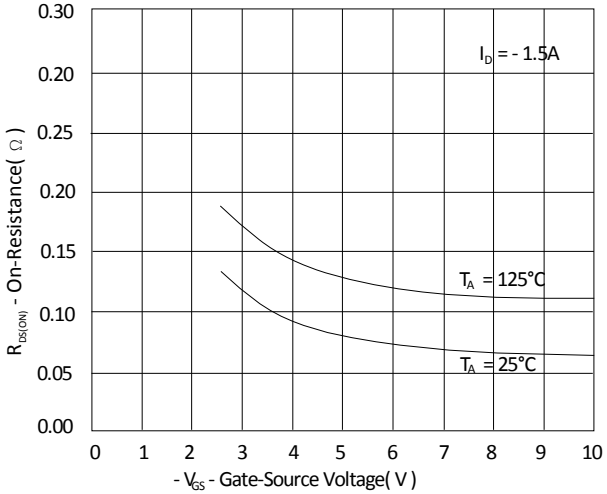
On-Resistance Variation with Drain Current and Gate Voltage



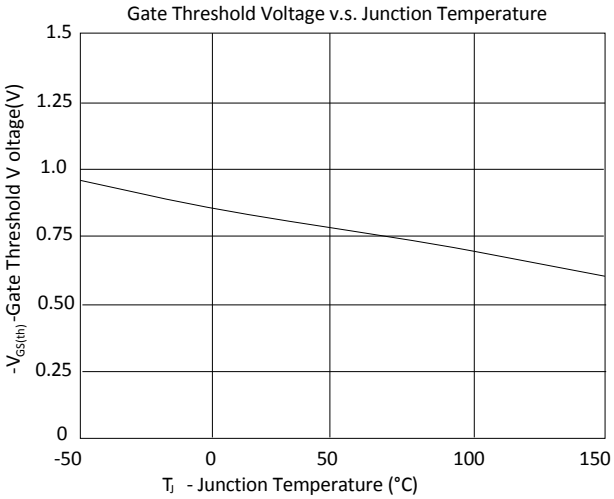
Normalized on-Resistance v.s. Junction Temperature



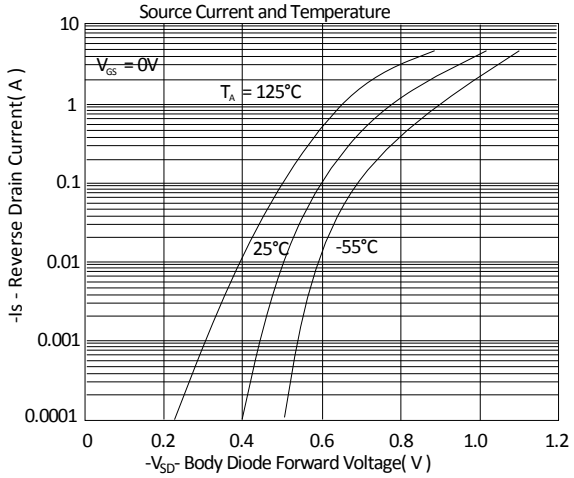
On-Resistance Variation with Gate-Source Voltage



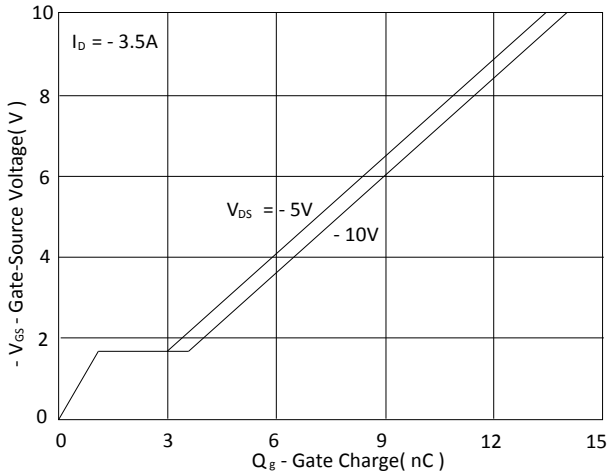
Gate Threshold Voltage v.s. Junction Temperature



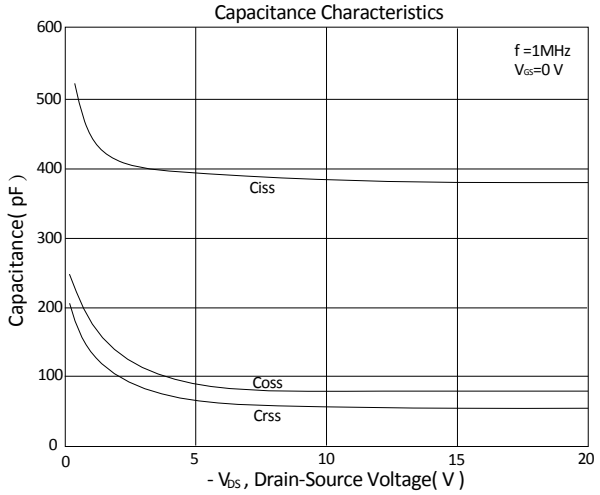
Body Diode Forward Voltage Variation with Source Current and Temperature



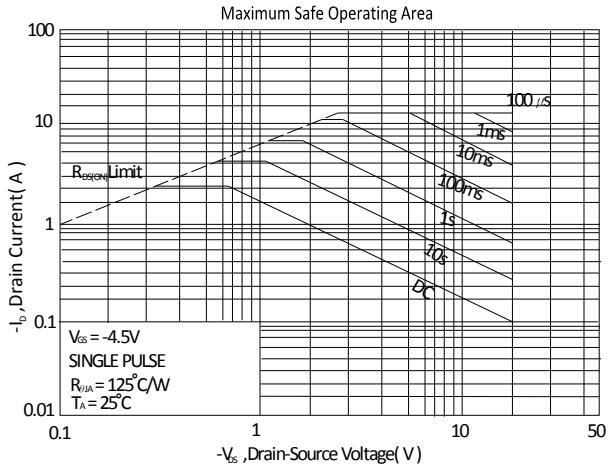
Gate Charge Characteristics



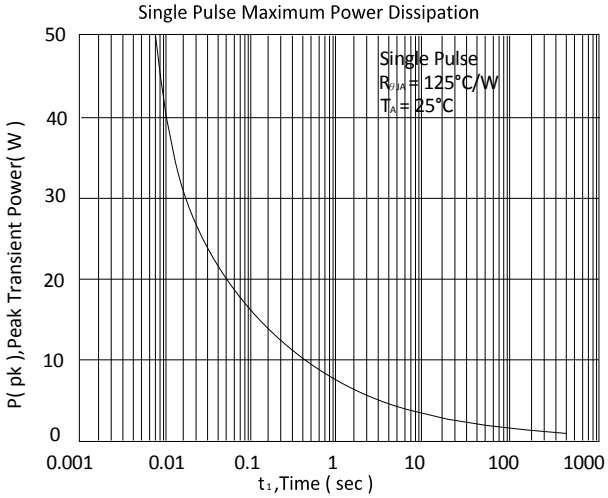
Capacitance Characteristics



Maximum Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve