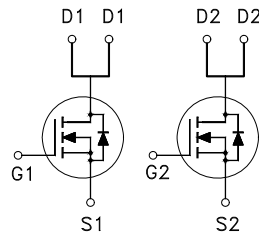


Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	30V
R _{DS(on)} (MAX.)	21mΩ
I _D	9A



UIS, R_g 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _A = 25 °C	I _D	9	A
	T _A = 100 °C		6.3	
Pulsed Drain Current ¹		I _{DM}	36	
Avalanche Current		I _{AS}	10	mJ
Avalanche Energy	L = 0.1mH, I _D =10A, R _G =25Ω	E _{AS}	5	
Repetitive Avalanche Energy ²	L = 0.05mH	E _{AR}	2.5	
Power Dissipation	T _A = 25 °C	P _D	2.27	W
	T _A = 100 °C		0.9	
Operating Junction & Storage Temperature Range		T _j , T _{stg}	-55 to 150	°C

100% UIS testing in condition of V_D=15V, L=0.1mH, V_G=10V, I_L=7.5A, Rated V_{DS}=30V N-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}		7.5	°C / W
Junction-to-Ambient ³	R _{θJA}		55	

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

³55°C / W when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_j = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1	1.5	3	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 24V, V _{GS} = 0V			1	μA
		V _{DS} = 20V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	9			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 10V, I _D = 9A		17	21	mΩ
		V _{GS} = 4.5V, I _D = 5A		24	32	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 9A		16		S
DYNAMIC						
Input Capacitance	C _{iSS}	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		520		pF
Output Capacitance	C _{oSS}			88		
Reverse Transfer Capacitance	C _{rSS}			62		
Gate Resistance	R _g	V _{GS} = 15mV, V _{DS} = 0V, f = 1MHz		2.0		Ω
Total Gate Charge ^{1,2}	Q _g (V _{GS} =10V)	V _{DS} = 15V, V _{GS} = 10V, I _D = 9A		11.5		nC
	Q _g (V _{GS} =4.5V)			5		
Gate-Source Charge ^{1,2}	Q _{gs}			1.6		
Gate-Drain Charge ^{1,2}	Q _{gd}			2.8		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{DS} = 15V, I _D = 1A, V _{GS} = 10V, R _{GS} = 6Ω		9		nS
Rise Time ^{1,2}	t _r			12		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			30		
Fall Time ^{1,2}	t _f			15		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _c = 25 °C)						
Continuous Current	I _S				2.3	A
Pulsed Current ³	I _{SM}				9.2	
Forward Voltage ¹	V _{SD}	I _F = I _S , V _{GS} = 0V			1.2	V
Reverse Recovery Time	t _{rr}	I _F = I _S , dI _F /dt = 100A / μS		50		nS
Peak Reverse Recovery Current	I _{RM(REC)}			30		A
Reverse Recovery Charge	Q _{rr}			2		nC

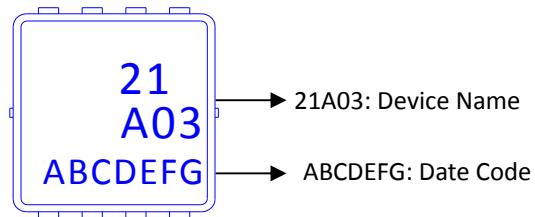
¹Pulse test : Pulse Width $\leq 300\mu$ sec, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

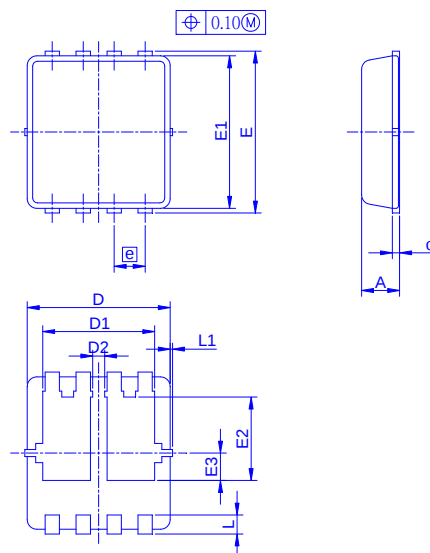
³Pulse width limited by maximum junction

temperature. **Ordering & Marking Information:**

Device Name: LB21N03BD for EDFN 3 x 3



Outline Drawing



Dimension in mm

Dimension	A	A1	b	c	D	D1	D2	E	E1	E2	E3	e	L	L1	$\theta 1$
Min.	0.70	0	0.24	0.10	2.95	2.25		3.15	2.95	1.65			0.30	0	0°
Typ.	0.80		0.30	0.152	3.00	2.35	0.225	3.20	3.00	1.75	0.575	0.65	0.40		10°
Max.	0.90	0.05	0.35	0.25	3.05	2.45		3.25	3.05	1.85			0.50	0.10	12°

Recommended minimum pads

