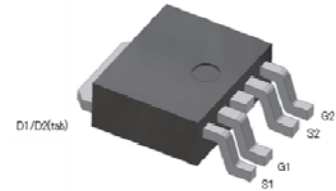
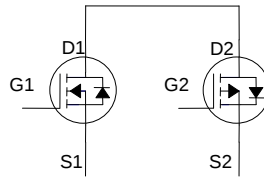


N & P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

	N-CH	P-CH
BV_{DSS}	30V	-30V
$R_{DS(on)} (MAX.)$	21m Ω	40m Ω
I_D	8A	-6A



UIS, 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
Gate-Source Voltage		V_{GS}	N-CH	P-CH	V
			±20	±20	
Continuous Drain Current	$T_C = 25\text{ }^{\circ}\text{C}$	I_D	8	-6	A
	$T_C = 100\text{ }^{\circ}\text{C}$		6	-5	
Pulsed Drain Current ¹		I_{DM}	32	-24	
Avalanche Current		I_{AS}	15	-15	
Avalanche Energy	L = 0.1mH, ID=10A, RG=25Ω (N) L = 0.1mH, ID=-10A, RG=25Ω (P)	E_{AS}	5	5	mJ
Repetitive Avalanche Energy ²	L = 0.05mH	E_{AR}	2.5	2.5	
Power Dissipation	$T_C = 25\text{ }^{\circ}\text{C}$	P_D	21		W
	$T_C = 100\text{ }^{\circ}\text{C}$		8.3		
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C

100% UIS testing in condition of $V_D=15V$, $L=0.1mH$, $V_G=10V$, $I_L=8A$, Rated $V_{DS}=30V$ N-CH

100% UIS testing in condition of $V_D=15V$, $L=0.1mH$, $V_G=-10V$, $I_L=-6A$, Rated $V_{DS}=-30V$ P-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		6	$^\circ\text{C} / \text{W}$
Junction-to-Ambient ³	$R_{\theta JA}$		42	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³90°C / W when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_c = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT	
			MIN	TYP	MAX		
STATIC							
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	N-CH	30			V
		V _{GS} = 0V, I _D = -250μA	P-CH	-30			
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	N-CH	1	1.5	3	
		V _{DS} = V _{GS} , I _D = -250μA	P-CH	-1	-1.5	-3	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V	N-CH			±100	nA
		V _{DS} = 0V, V _{GS} = ±20V	P-CH			±100	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 24V, V _{GS} = 0V	N-CH			1	μA
		V _{DS} = -24V, V _{GS} = 0V	P-CH			-1	
		V _{DS} = 20V, V _{GS} = 0V, T _J = 125 °C	N-CH			25	
		V _{DS} = -20V, V _{GS} = 0V, T _J = 125 °C	P-CH			-25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	N-CH	8			A
		V _{DS} = -5V, V _{GS} = -10V	P-CH	-6			
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 10V, I _D = 8A	N-CH		17	21	mΩ
		V _{GS} = -10V, I _D = -6A	P-CH		35	40	
		V _{GS} = 4.5V, I _D = 6A	N-CH		25	30	
		V _{GS} = -4.5V, I _D = -5A	P-CH		55	65	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 8A	N-CH		16		S
		V _{DS} = -5V, I _D = -6A	P-CH		16		
DYNAMIC							
Input Capacitance	C _{iss}	N-CH V _{GS} = 0V, V _{DS} = 15V, f = 1MHz P=CH V _{GS} = 0V, V _{DS} = -15V, f = 1MHz	N-CH		520		pF
			P-CH		820		
Output Capacitance	C _{oss}		N-CH		88		
			P-CH		122		
Reverse Transfer Capacitance	C _{rss}		N-CH		62		
			P-CH		97		

Total Gate Charge ^{1,2}	Q _g (V _{GS} =10V)	N-CH V _{DS} = 15V, V _{GS} = 10V, I _D = 8A P-CH V _{DS} = -15V, V _{GS} = -10V, I _D = -6A	N-CH		11.5		nC
	Q _g (V _{GS} =-10V)		P-CH		9		
	Q _g (V _{GS} =4.5V)		N-CH		5		
	Q _g (V _{GS} =-4.5V)		P-CH		5.8		
Gate-Source Charge ^{1,2}	Q _{gs}		N-CH		1.6		nS
Gate-Drain Charge ^{1,2}	Q _{gd}		P-CH		2.2		
Turn-On Delay Time ^{1,2}	t _{d(on)}		N-CH		11		
			P-CH		10		
Rise Time ^{1,2}	t _r	I _D = 1A, V _{GS} = 10V, R _{GS} = 6Ω P-CH	N-CH		16		nS
Turn-Off Delay Time ^{1,2}	t _{d(off)}	V _{DS} = -15V, I _D = -1A, V _{GS} = -10V, R _{GS} = 6Ω	P-CH		15		
		N-CH		36			
Fall Time ^{1,2}	t _f		P-CH		28		
		N-CH		20			
			P-CH		15		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _c = 25 °C)							
Continuous Current	I _S		N-CH			2.3	A
			P-CH			-2.3	
Pulsed Current ³	I _{SM}		N-CH			9.2	A
			P-CH			-9.2	
Forward Voltage ¹	V _{SD}	I _F = I _S , V _{GS} = 0V	N-CH			1.2	V
			P-CH			-1.2	
Reverse Recovery Time	t _{rr}	I _F = I _S , dI _F /dt = 100A / μS	N-CH		50		nS
			P-CH		55		
Peak Reverse Recovery Current	I _{RM(REC)}		N-CH		30		A
			P-CH		-22		
Reverse Recovery Charge	Q _{rr}		N-CH		2		nC
			P-CH		2.1		

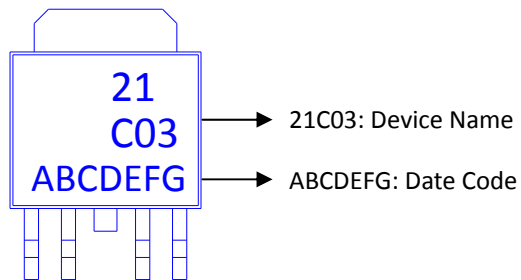
¹Pulse test : Pulse Width $\leq 300 \mu sec$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

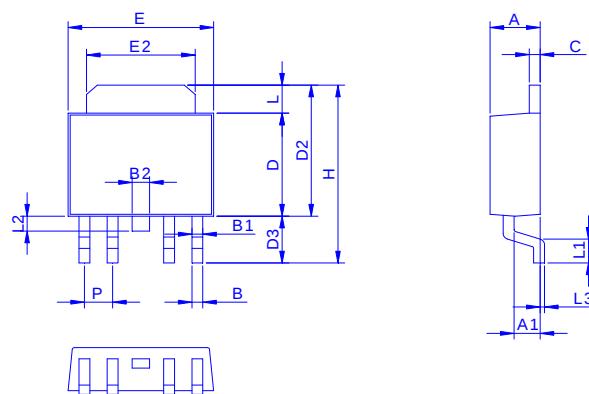
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: LB21C03D for DPAK (TO-252)

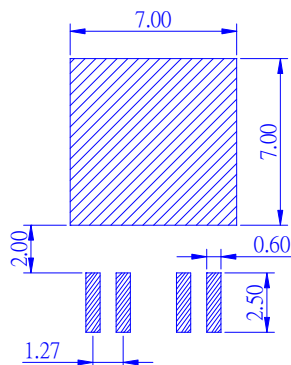


Outline Drawing

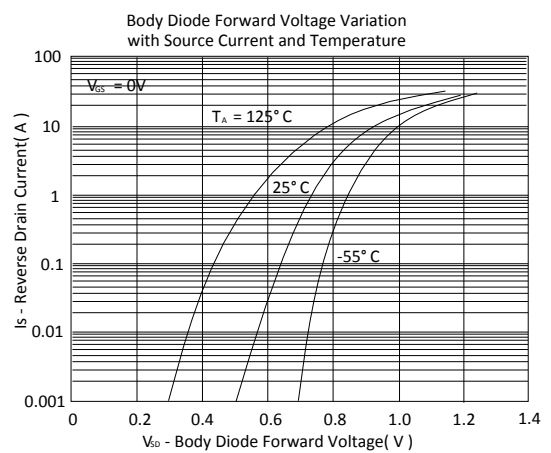
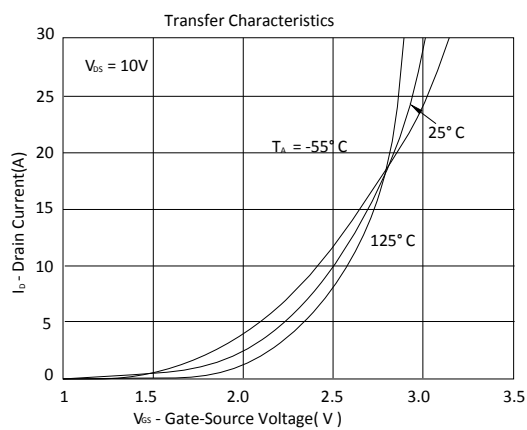
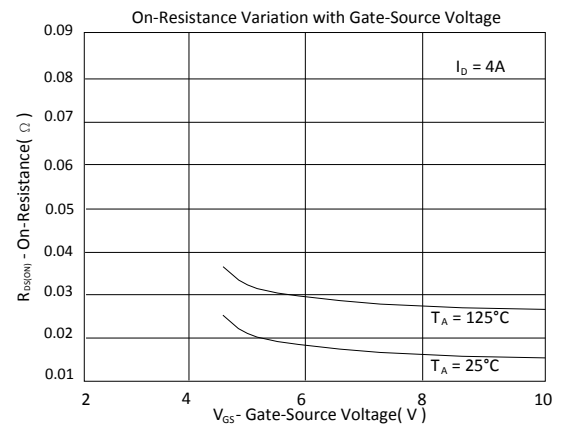
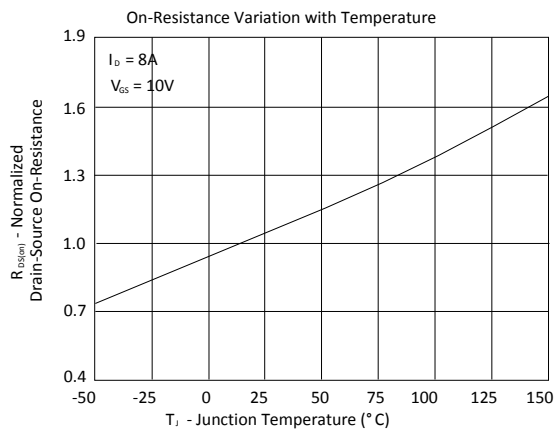
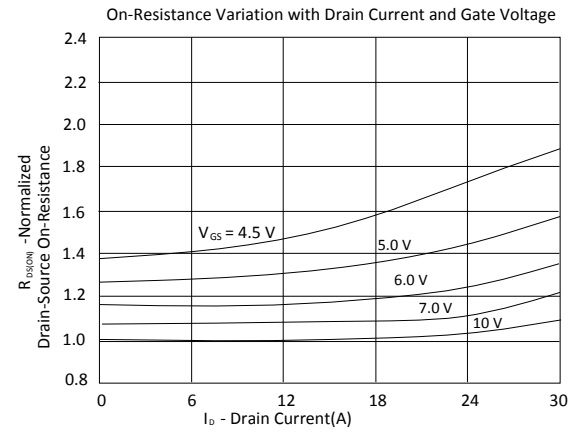
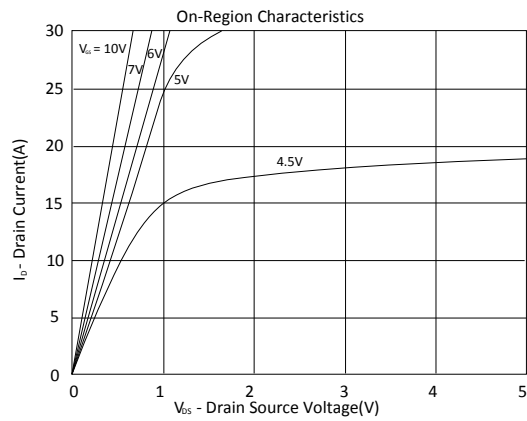


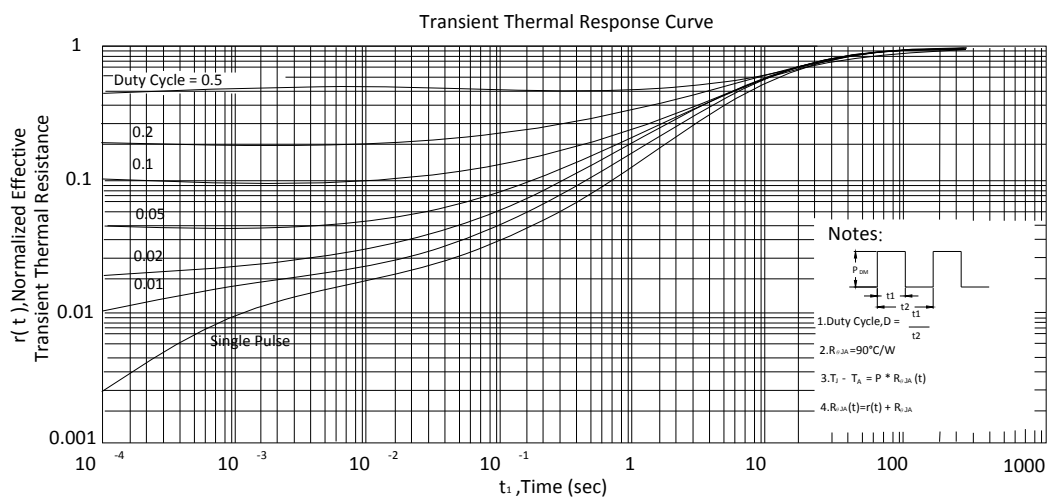
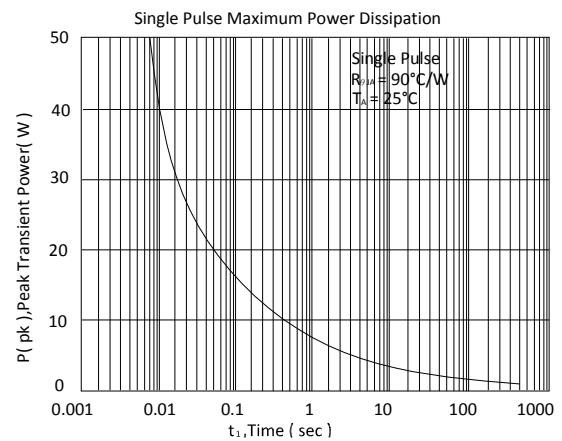
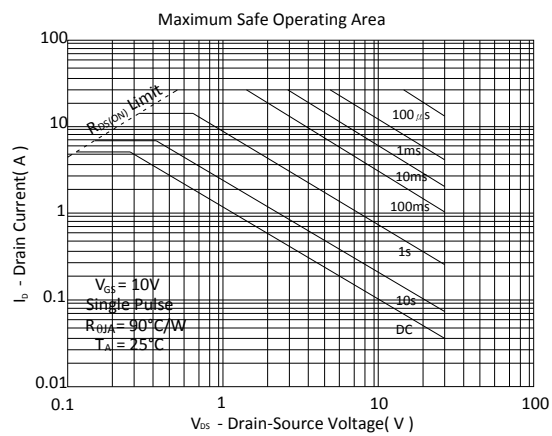
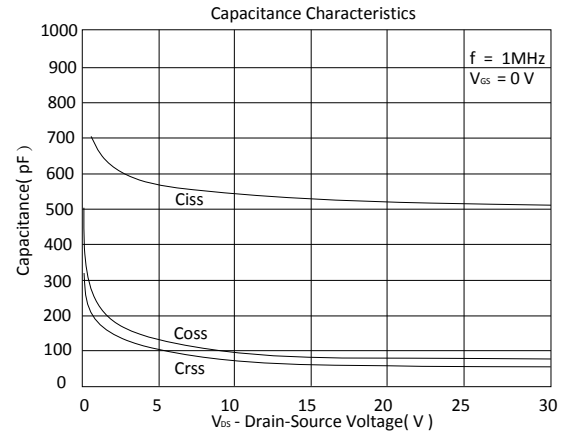
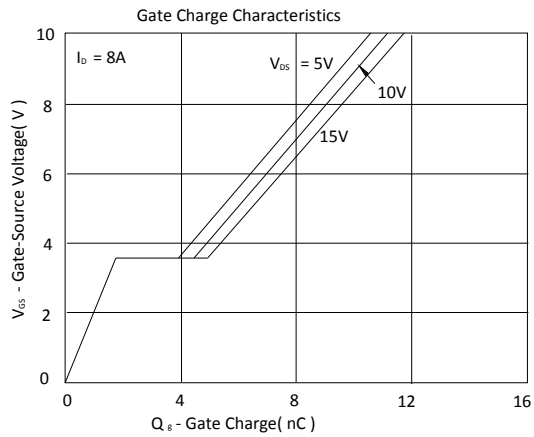
Dimension in mm

Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	1.10	0.30	0.55	0.40	0.40	5.30	6.70	2.20	6.30	4.80	9.20	1.30	0.90	0.50	0.00	1.17
Max.	2.50	1.30	0.70	0.75	0.80	0.60	5.70	7.30	3.00	6.70	5.45	10.15	1.70	1.50	1.10	0.30	1.37



N-Channel





P-Channel

