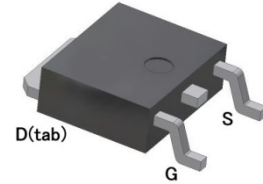


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	250V
R _{DS(on)} (MAX.)	1 Ω
I _D	4.4A



UIS, R_g 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _C = 25 °C	I _D	4.4	A
	T _C = 100 °C		2.6	
Pulsed Drain Current ¹		I _{DM}	17.6	
Avalanche Current		I _{AS}	1	mJ
Avalanche Energy	L = 3mH, I _D =1A, R _G =25 Ω	E _{AS}	1.5	
Repetitive Avalanche Energy ²	L = 1mH	E _{AR}	0.5	
Power Dissipation	T _C = 25 °C	P _D	29	W
	T _C = 100 °C		11	
Operating Junction & Storage Temperature Range		T _j , T _{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}		4.2	°C / W
Junction-to-Ambient	R _{θJA}		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS (T_c = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 10mA	250			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1	2	3	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 200V, V _{GS} = 0V			1	μA
		V _{DS} = 200V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	4.4			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 10V, I _D = 2.2A		0.82	1.0	Ω
		V _{GS} = 5V, I _D = 1.1A		0.90	1.1	
Forward Transconductance ¹	g _{fs}	V _{DS} = 50V, I _D = 2.2A		2.3		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 25V, f = 1MHz		1224		pF
Output Capacitance	C _{oss}			27		
Reverse Transfer Capacitance	C _{rss}			23		
Gate Resistance	R _g	V _{GS} = 15mV, V _{DS} = 0V, f = 1MHz		2.0		Ω
Total Gate Charge ^{1,2}	Q _g	V _{DS} = 200V, V _{GS} = 10V, I _D = 2.2A		32		nC
Gate-Source Charge ^{1,2}	Q _{gs}			4		
Gate-Drain Charge ^{1,2}	Q _{gd}			8.1		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{DS} = 125V, I _D = 1A, V _{GS} = 10V, R _G = 6Ω		10		nS
Rise Time ^{1,2}	t _r			65		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			20		
Fall Time ^{1,2}	t _f			35		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _C = 25 °C)						
Continuous Current	I _S				4.4	A
Pulsed Current ³	I _{SM}				17.6	
Forward Voltage ¹	V _{SD}	I _F = I _S , V _{GS} = 0V			1.3	V
Reverse Recovery Time	t _{rr}	I _F = 4.4A, dI _F /dt = 100A / μS		125		nS
Reverse Recovery Charge	Q _{rr}			500		nC

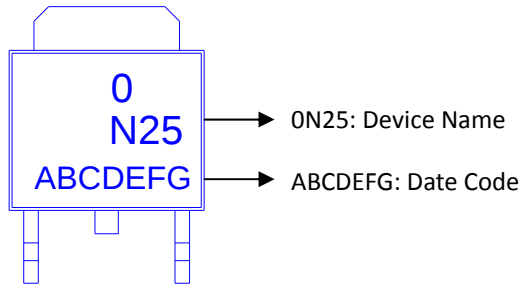
¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

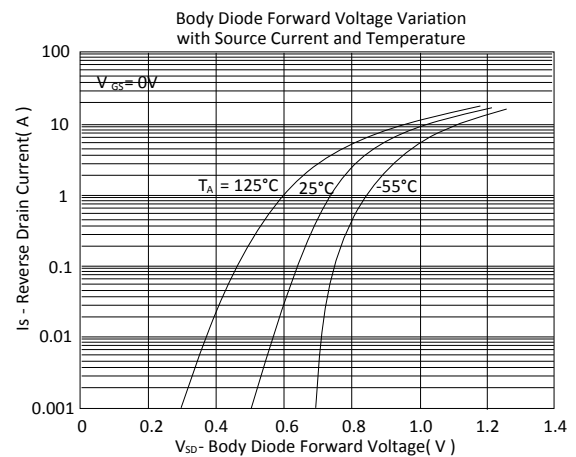
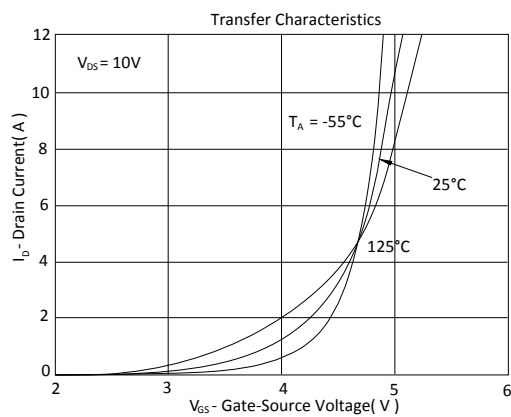
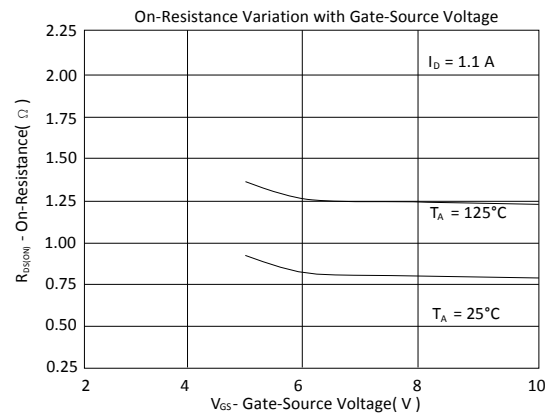
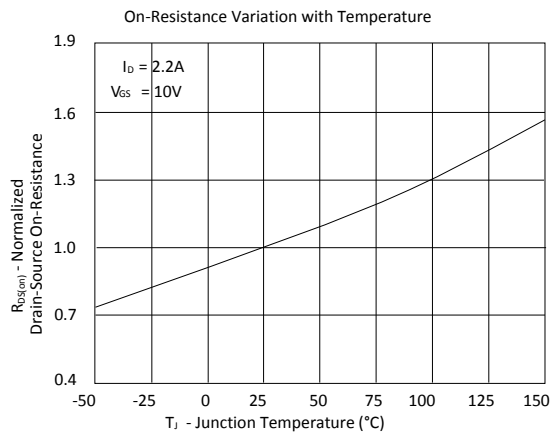
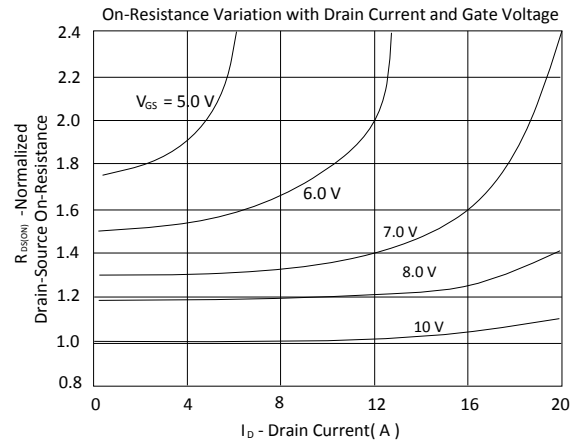
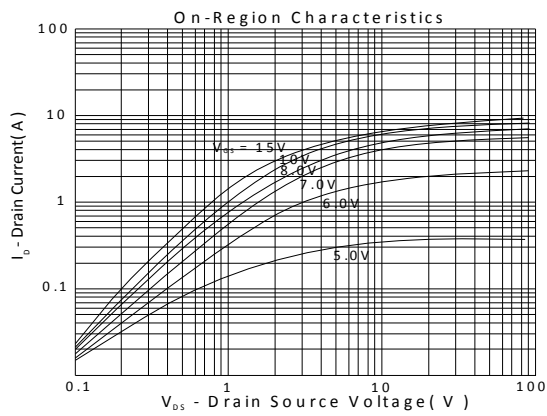
³Pulse width limited by maximum junction temperature.

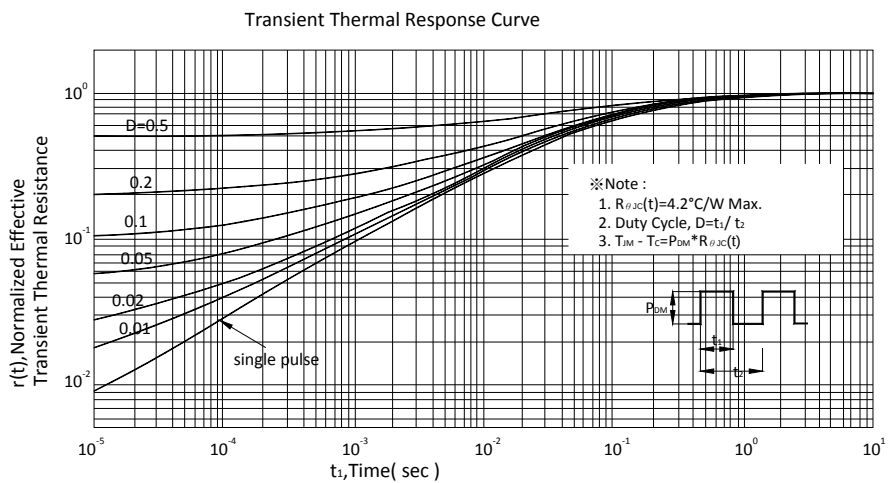
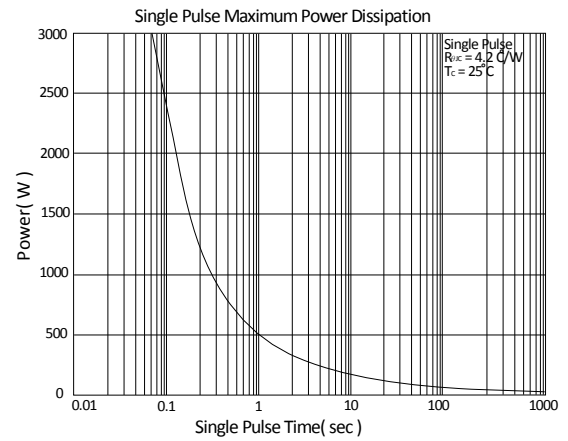
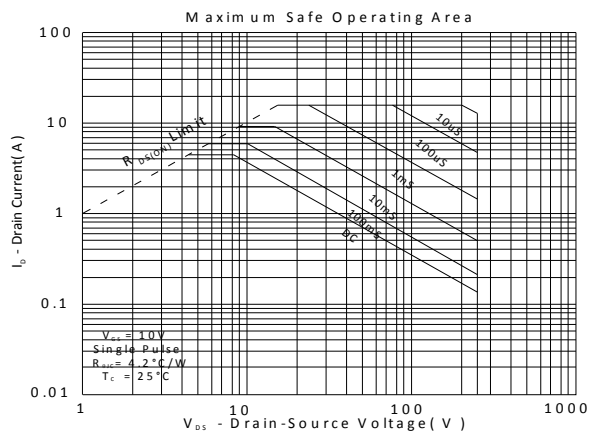
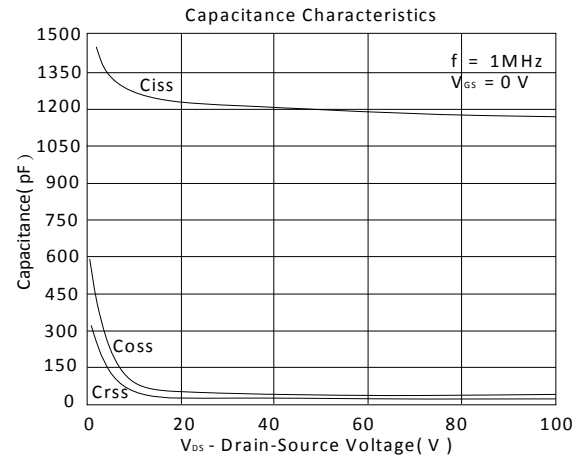
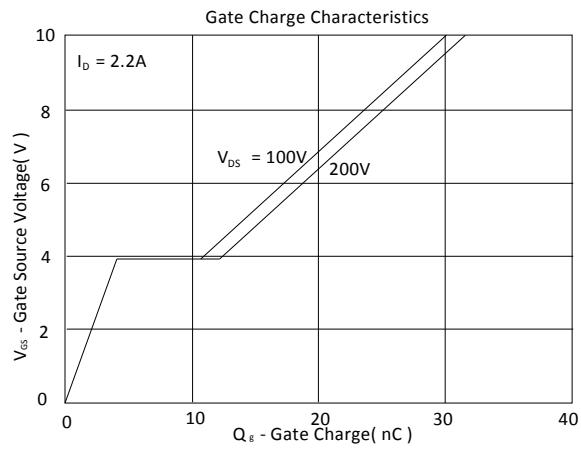
Ordering & Marking Information:

Device Name: LB0N25D for DPAK (TO-252)

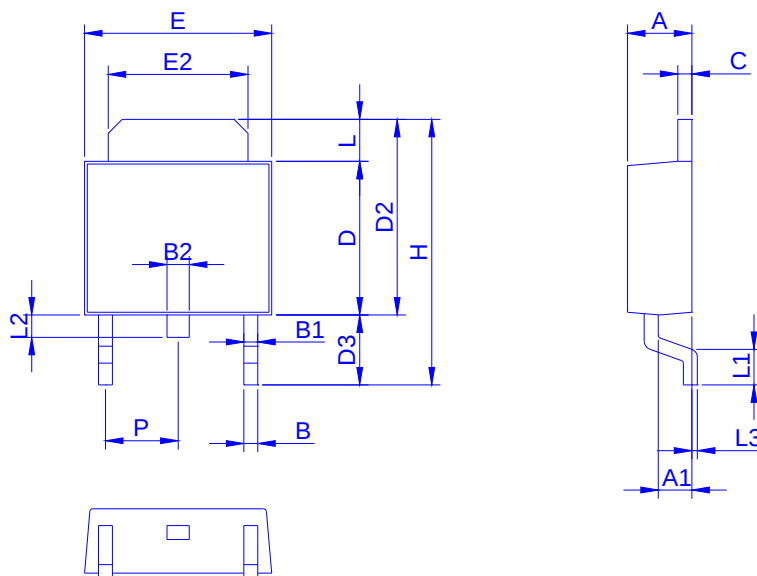


TYPICAL CHARACTERISTICS





Outline Drawing



Dimension in mm

Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	0.95	0.30	0.40	0.60	0.40	5.30	6.70	2.20	6.40	4.80	9.20	0.89	0.90	0.50	0.00	2.10
Max.	2.50	1.30	0.85	0.94	1.00	0.60	6.20	7.30	3.00	6.70	5.45	10.15	1.70	1.65	1.10	0.30	2.50

Footprint

