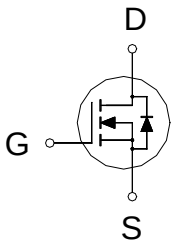
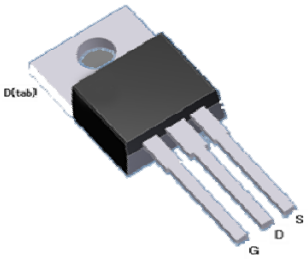
N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	75V
$R_{DSON\ (MAX.)}$	9mΩ
I_D	103A





UIS, Rg 100% Tested

Pb-Free Lead Plating

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current	T_C = 25 °C	I_D	103	A
	T_C = 100 °C		80	
Pulsed Drain Current[1]		I_{DM}	200	
Avalanche Current		I_{AS}	68	
Avalanche Energy	L = 0.3mH, ID=60A, RG=25Ω	E_{AS}	540	mJ
Repetitive Avalanche Energy[2]	L = 0.1mH	E_{AR}	180	
Power Dissipation	T_C = 25 °C	P_D	223	W
	T_C = 100 °C		89	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		0.56	°C / W
Junction-to-Ambient	$R_{\theta JA}$		60	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	75			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	3.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±30V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V			1	μA
		V_{DS} = 50V, V_{GS} = 0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	103			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 30A		7.5	9	mΩ
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 30A		40		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 40V, f = 1MHz		2760		pF
Output Capacitance	C_{oss}			288		
Reverse Transfer Capacitance	C_{rss}			49		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz		2.8		Ω
Total Gate Charge[1,2]	Q_g	V_{DS} = 40V, V_{GS} = 10V, I_D = 30A		37		nC
Gate-Source Charge[1,2]	Q_{gs}			15		
Gate-Drain Charge[1,2]	Q_{gd}			10		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = 40V, I_D = 1A, V_{GS} = 10V, R_{GS} = 6Ω		25		nS
Rise Time[1,2]	t_r			100		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			100		
Fall Time[1,2]	t_f			120		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				103	A
Pulsed Current[3]	I_{SM}				200	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			1.3	V
Reverse Recovery Time	t_{rr}	I_F = 25A, dI_F/dt = 100A / μS		130		nS
Reverse Recovery Charge	Q_{rr}			400		nC

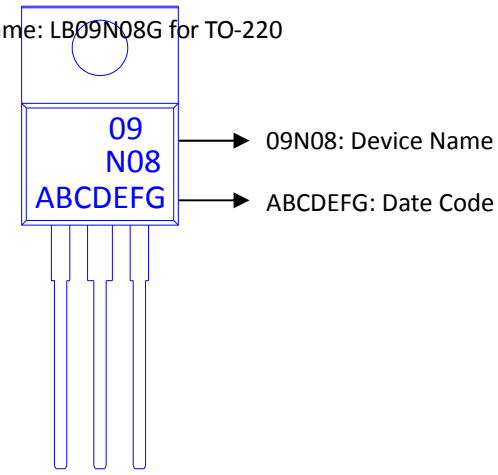
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

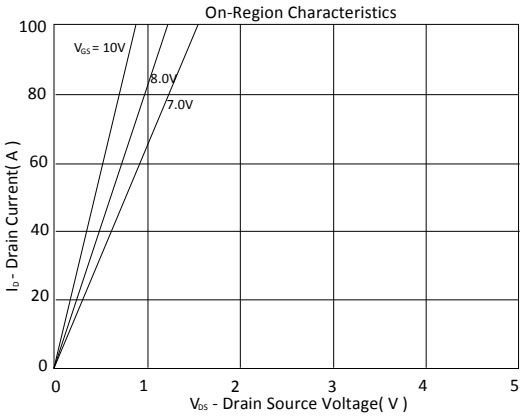
[3]Pulse width limited by maximum junction temperature.

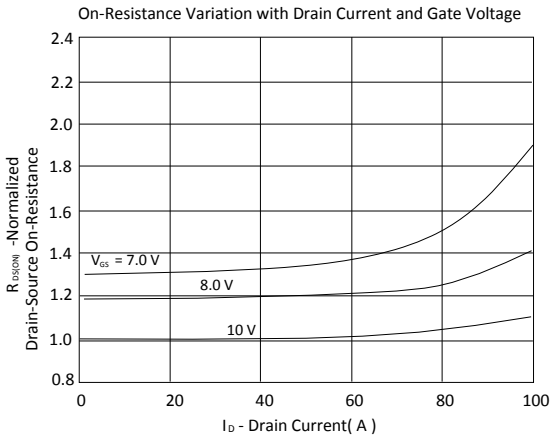
Ordering & Marking Information:

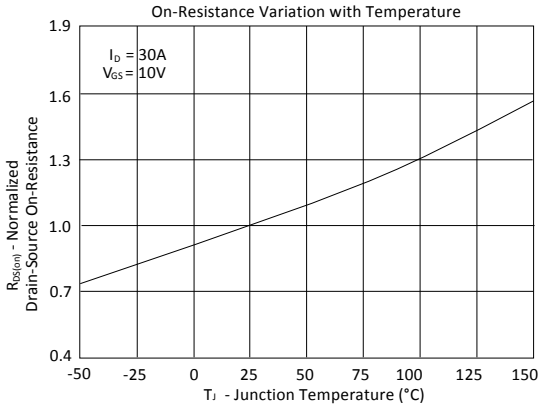
Device Name: LB09N08G for TO-220

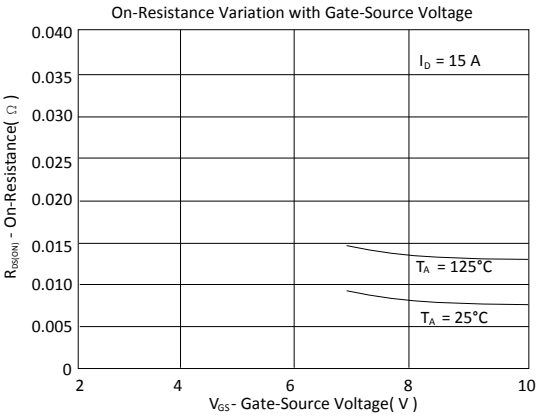


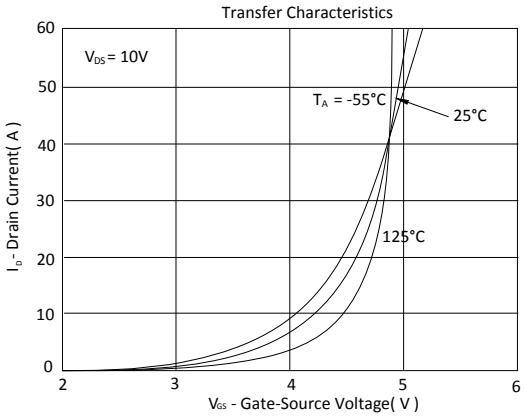
TYPICAL CHARACTERISTICS

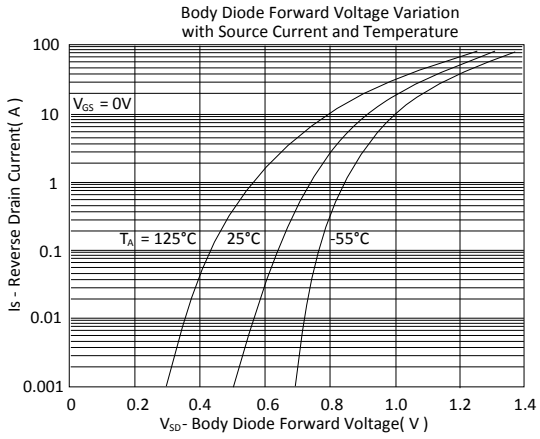




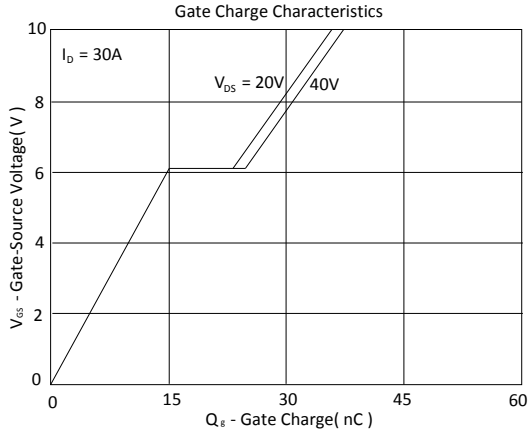




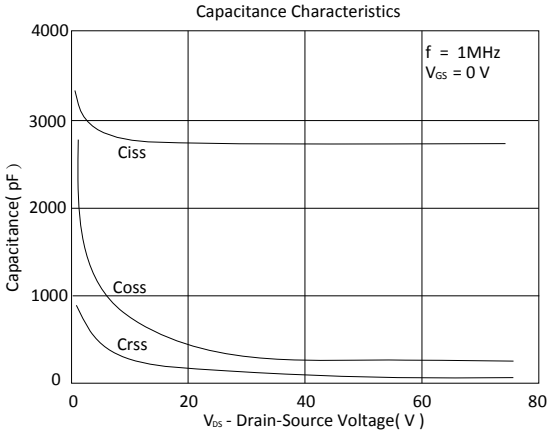




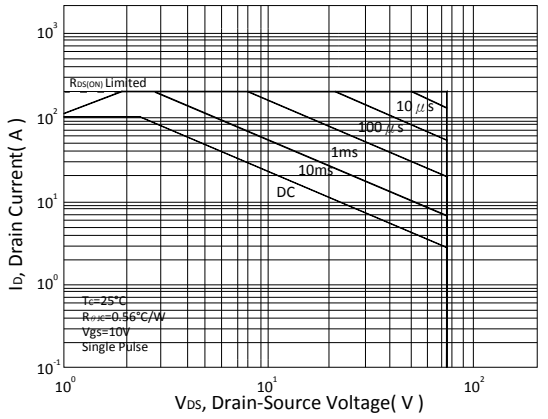
Gate Charge Characteristics



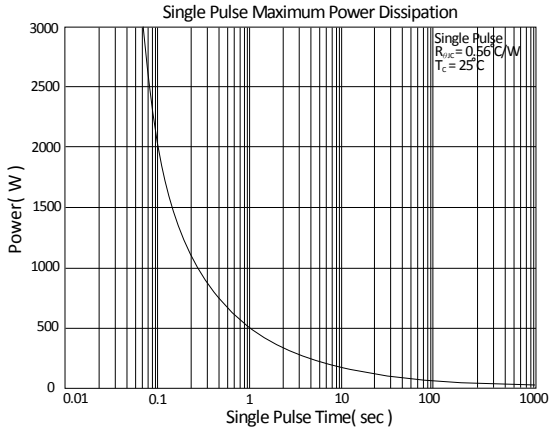
Capacitance Characteristics



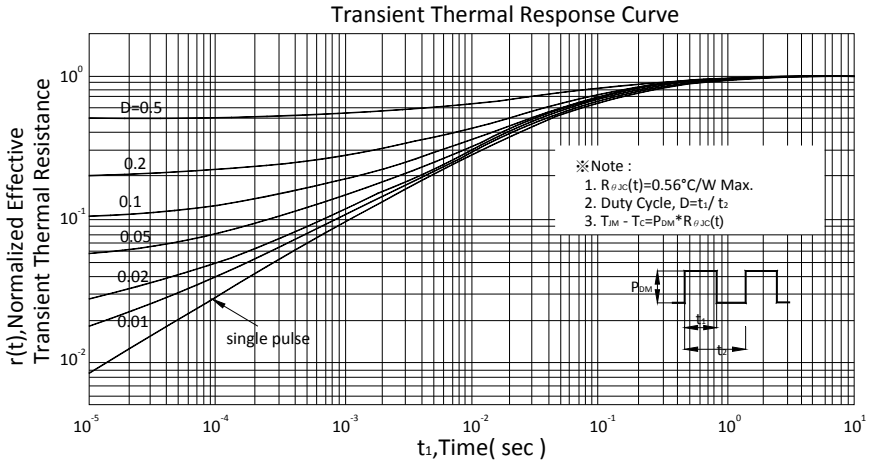
Maximum Safe Operating Area



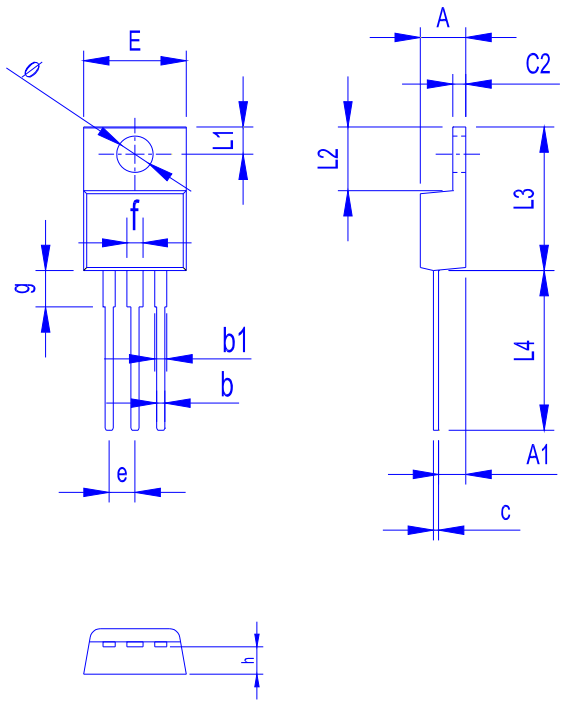
Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



Outline Drawing



Dimension in mm

Dimension	A	b	b1	c	c2	E	L1	L2	L3	L4	ø	e	f	g	h
Min.	4.20	0.70	0.90	0.30	1.10	9.80	2.55	6.10	14.80	13.50	3.40	2.35	1.30	3.40	2.40
Max.	4.80	1.10	1.50	0.70	1.50	10.50	2.85	6.50	15.40	14.50	3.80	2.75	1.90	3.80	3.00