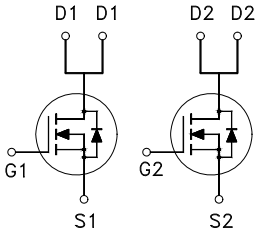
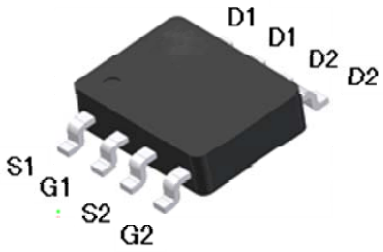
N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

	N-CH-Q1	N-CH-Q2
BV_{DSS}	40V	40V
$R_{DSON\ (MAX.)}$	17.5mΩ	8.8mΩ
I_D	7.4A	10.5A





UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

GP
GREEN PRODUCT

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
			Q1	Q2	
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current	T_A = 25 °C	I_D	7.4	10.5	A
	T_A = 70 °C		5.6	8.4	
Pulsed Drain Current[1]		I_{DM}	30	42	
Avalanche Current		I_{AS}	7.5	10.5	
Avalanche Energy	L = 0.1mH, R_G=25Ω	E_{AS}	2.8	5.5	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	E_{AR}	1.4	2.7	
Power Dissipation	T_A = 25 °C	P_D	2		W
	T_A = 100 °C		0.8		
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		25	°C / W
Junction-to-Ambient[3]	$R_{\theta JA}$		62.5	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

[3]62.5°C / W when mounted on a 1 in^2 pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS			UNIT
				MIN	TYP	MAX	
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	Q1	40			V
			Q2	40			
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	Q1	1	1.7	3	
			Q2	1	1.7	3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	Q1			±100	nA
			Q2			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 32V, V_{GS} = 0V	Q1			1	μA
			Q2			1	
		V_{DS} = 30V, V_{GS} = 0V, T_J = 125 °C	Q1			25	
			Q2			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	Q1	7.4			A
			Q2	10.5			
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 6A	Q1		15.5	17.5	mΩ
		V_{GS} = 10V, I_D = 10A	Q2		8.0	8.8	
		V_{GS} = 4.5V, I_D = 4A	Q1		22	32	
		V_{GS} = 4.5V, I_D = 8A	Q2		11	15	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 6A	Q1		15		S
		V_{DS} = 5V, I_D = 10A	Q2		18		
DYNAMIC							
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 20V, f = 1MHz	Q1		707		pF
			Q2		1962		
Output Capacitance	C_{oss}		Q1		98		
			Q2		245		
Reverse Transfer Capacitance	C_{rss}		Q1		81		
			Q2		225		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz	Q1		1.5		Ω
			Q2		1.4		

Total Gate Charge[1,2]	Q_g(V_{GS}=10V)	Q1 V_{DD} = 20V, V_{GS} = 10V, I_D = 6A Q2 V_{DD} = 20V, V_{GS} = 10V, I_D = 10A	Q1		18		nC
			Q2		47		
	Q_g(V_{GS}=4.5V)		Q1		10		
			Q2		24		
Gate-Source Charge[1,2]	Q_{gs}		Q1		2.4		
			Q2		6.8		
Gate-Drain Charge[1,2]	Q_{gd}		Q1		6.0		
			Q2		16		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DD} = 20V, I_D = 1A, V_{GS} = 10V, R_{GS} = 2.7Ω	Q1		6		nS
			Q2		10		
Rise Time[1,2]	t_r		Q1		10		
			Q2		18		
Turn-Off Delay Time[1,2]	$t_{d(off)}$		Q1		18		
			Q2		20		
Fall Time[1,2]	t_f		Q1		12		
			Q2		15		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)							
Continuous Current	I_S		Q1			7.5	A
			Q2			10.5	
Pulsed Current[3]	I_{SM}		Q1			30	
			Q2			42	
Forward Voltage[1]	V_{SD}	I_F = 6A, V_{GS} = 0V I_F = 10A, V_{GS} = 0V	Q1			1.3	V
			Q2			1.3	
Reverse Recovery Time	t_{rr}	Q1 I_F = 6A, dI_F/dt = 100A / μS	Q1		18		nS
			Q2		22		
Reverse Recovery Charge	Q_{rr}	Q2 I_F = 10A, dI_F/dt = 100A / μS	Q1		5		nC
			Q2		6		

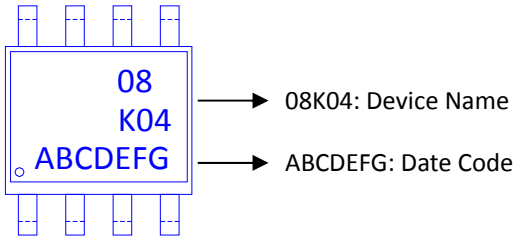
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

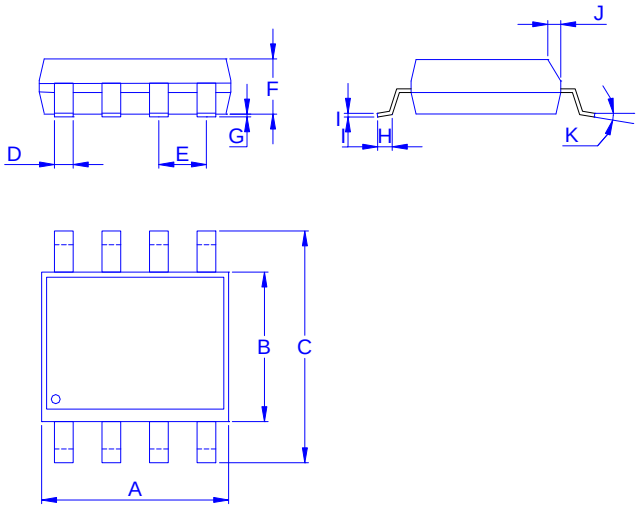
[3]Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: LB08N04HP for SOP-8



Outline Drawing

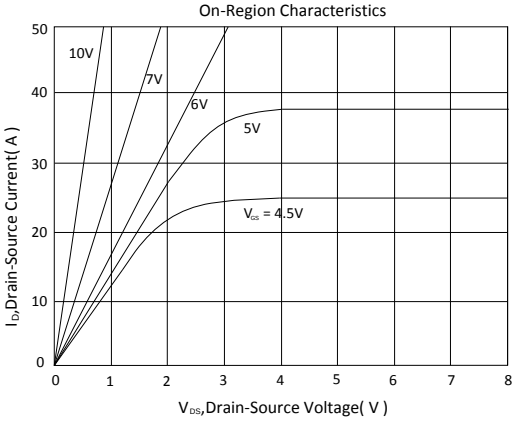


Dimension in mm

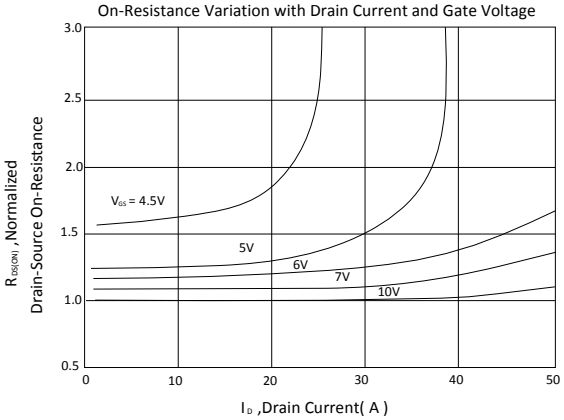
Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°

Q1 TYPICAL CHARACTERISTICS

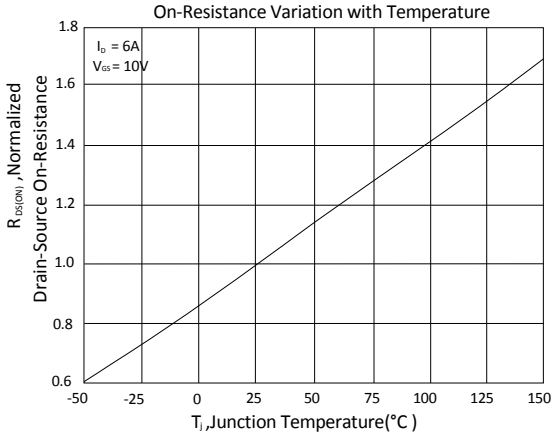
On-Region Characteristics



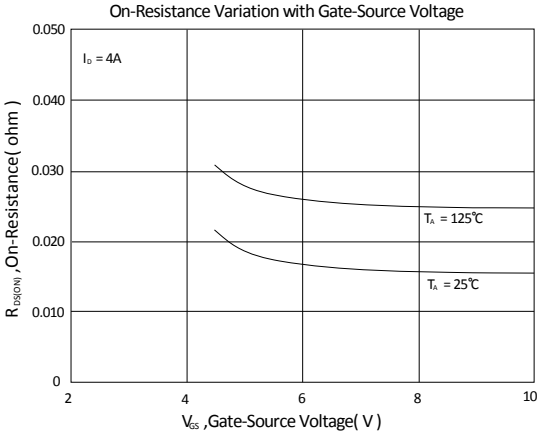
On-Resistance Variation with Drain Current and Gate Voltage



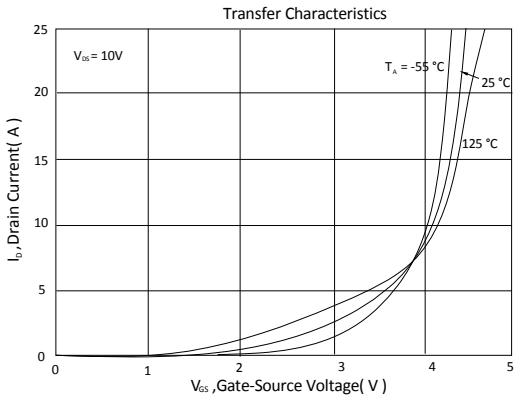
On-Resistance Variation with Temperature



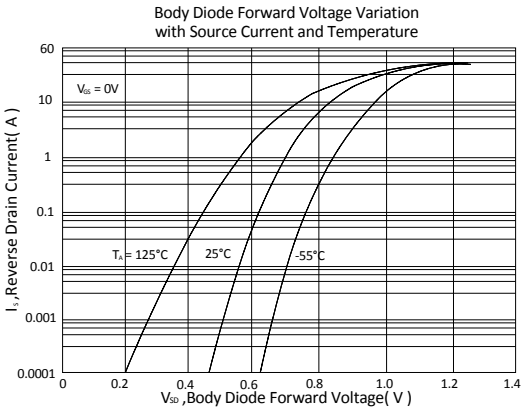
On-Resistance Variation with Gate-Source Voltage

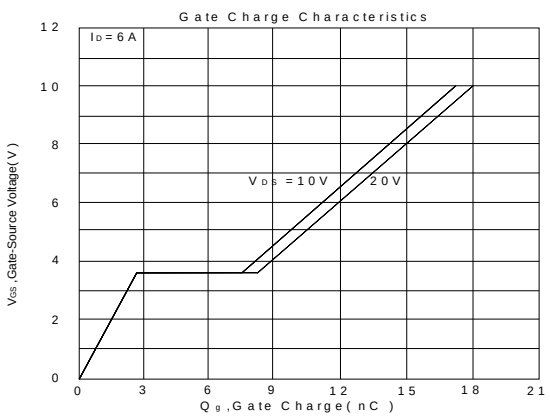


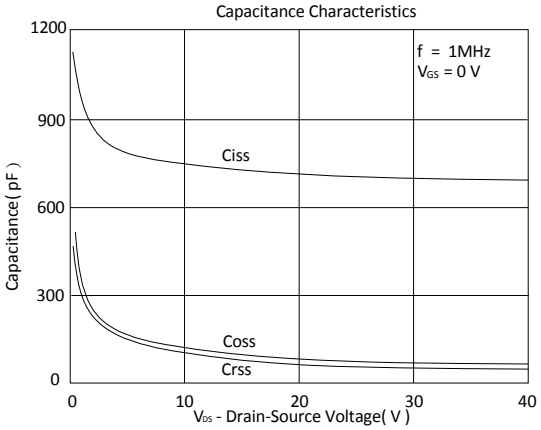
Transfer Characteristics

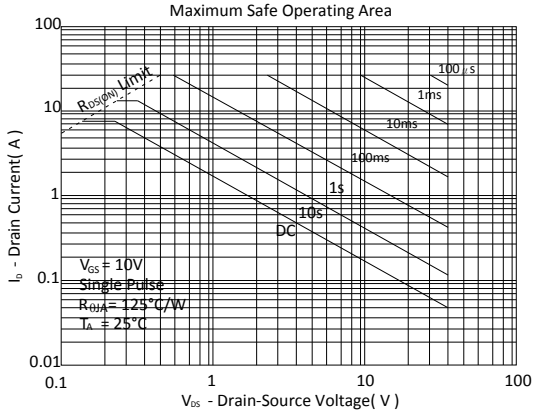


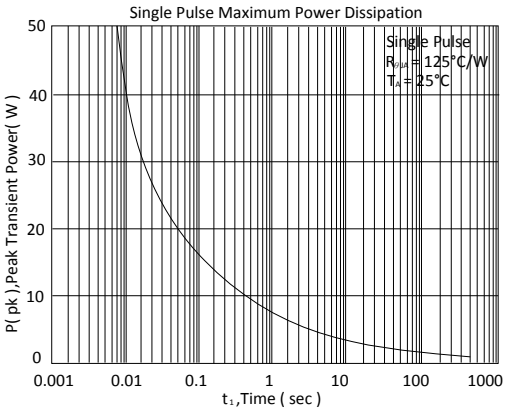
Body Diode Forward Voltage Variation
with Source Current and Temperature

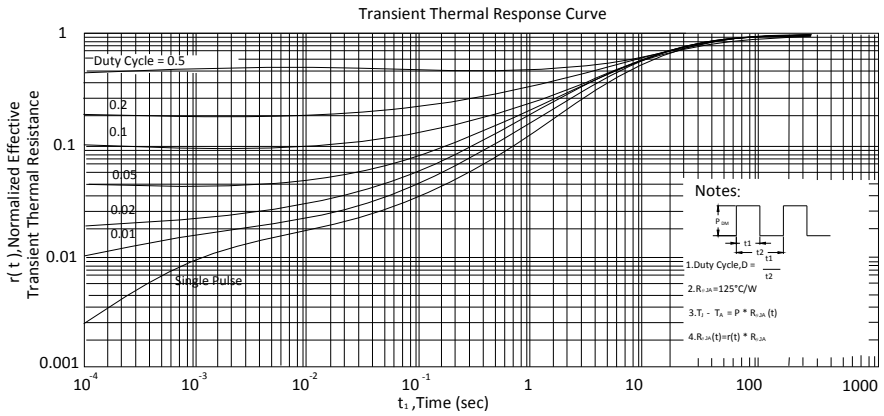



Gate Charge Characteristics
I D = 6 A
V D S = 1 0 V
2 0 V
V GS ,Gate-Source Voltage(V)
Q g ,G a t e C h a r g e (n C)

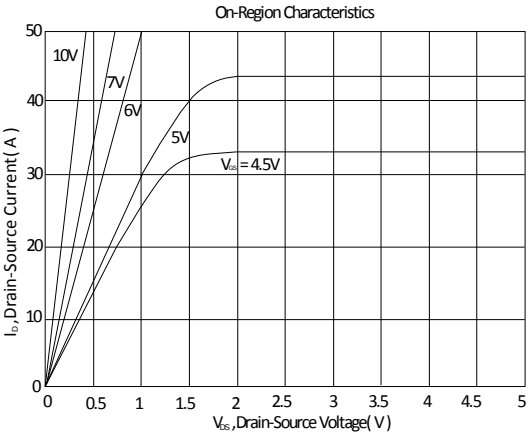

Capacitance Characteristics
f = 1MHz
VGS = 0 V
Ciss
Coss
Crss
Capacitance(pF)
VDS - Drain-Source Voltage(V)

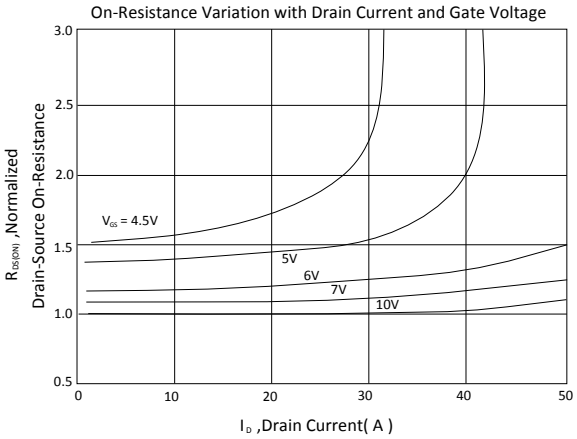

Maximum Safe Operating Area
RDS(ON) Limit
100μs
1ms
10ms
100ms
1s
10s
DC
VGS = 10V
Single Pulse
RθJA= 125°C/W
TA = 25°C
ID - Drain Current(A)
VDS - Drain-Source Voltage(V)

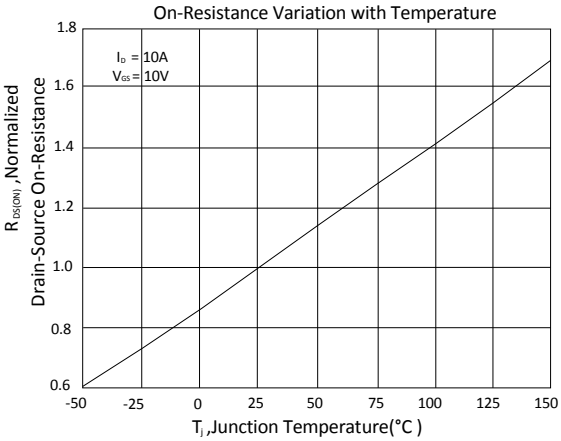

Single Pulse Maximum Power Dissipation
Single Pulse
RθJA = 125°C/W
TA = 25°C
P(pk),Peak Transient Power(W)
t1 ,Time (sec)

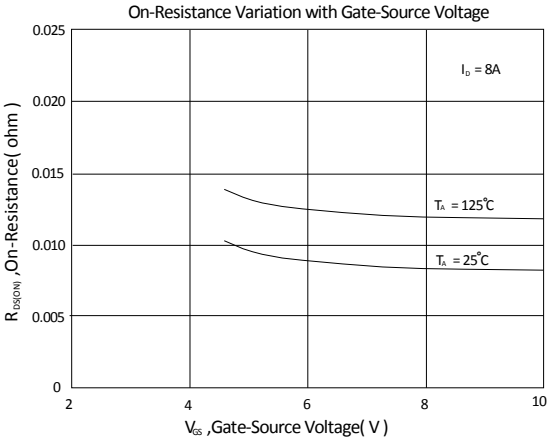

Transient Thermal Response Curve
Duty Cycle = 0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
Notes:
1.Duty Cycle,D =
2.RθJA=125°C/W
3.TJ - TA = P * RθJA (t)
4.RθJA(t)=r(t) * RθJA
r(t),Normalized Effective Transient Thermal Resistance
t1 ,Time (sec)

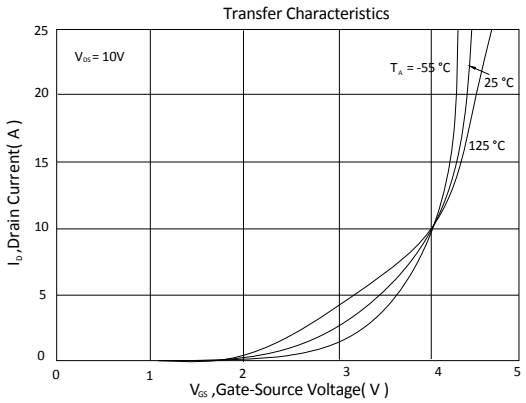
Q2 TYPICAL CHARACTERISTICS

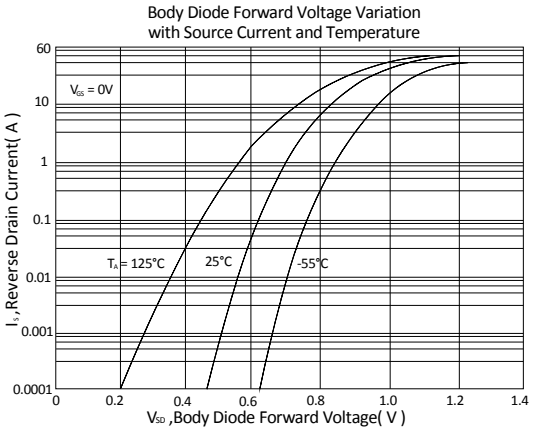


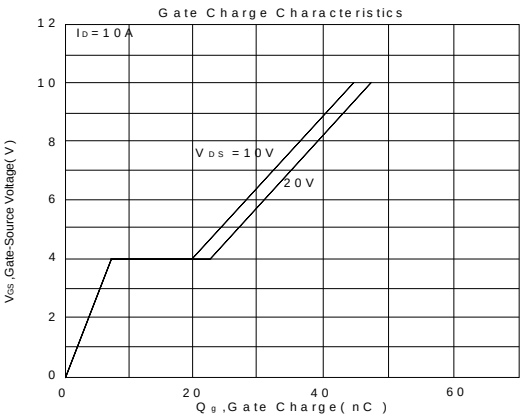


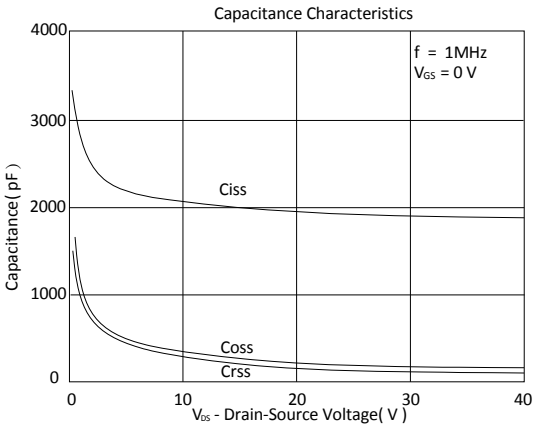


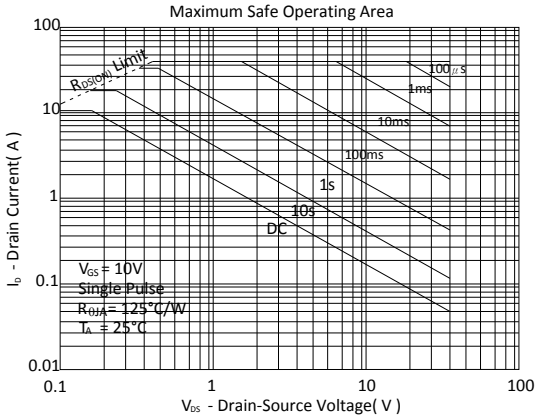


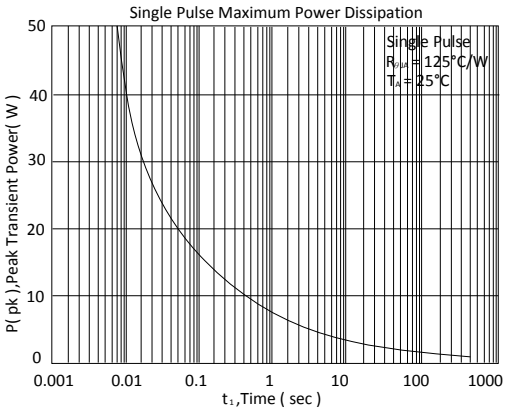


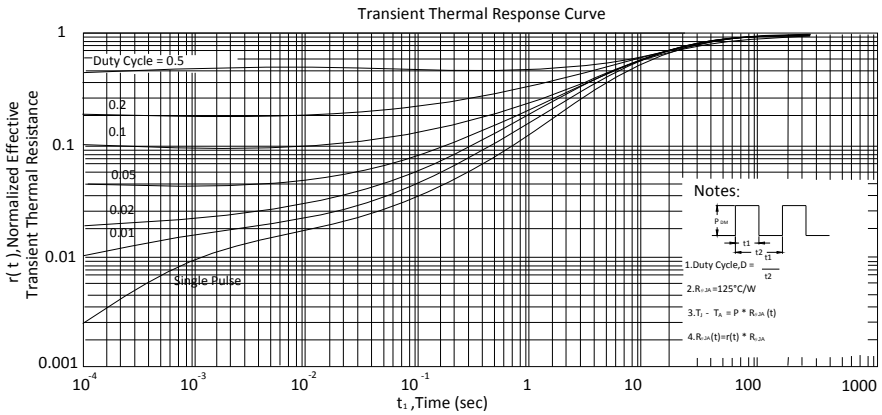



Gate Charge Characteristics
ID = 10A
VDS = 10V
20V
VGS ,Gate-Source Voltage(V)
Qg ,Gate Charge(nC)


Capacitance Characteristics
f = 1MHz
VGS = 0 V
Ciss
Coss
Crss
Capacitance(pF)
VDS - Drain-Source Voltage(V)


Maximum Safe Operating Area
RDS(on) Limit
100μs
1ms
10ms
100ms
1s
10s
DC
VGS = 10V
Single Pulse
RθJA= 125°C/W
TA = 25°C
ID - Drain Current(A)
VDS - Drain-Source Voltage(V)


Single Pulse Maximum Power Dissipation
Single Pulse
RθJA = 125°C/W
TA = 25°C
P(pk),Peak Transient Power(W)
t1 ,Time (sec)


Transient Thermal Response Curve
Duty Cycle = 0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
Notes:
1.Duty Cycle,D =
2.RθJA=125°C/W
3.TJ - TA = P * RθJA (t)
4.RθJA(t)=r(t) * RθJA
r(t),Normalized Effective Transient Thermal Resistance
t1 ,Time (sec)