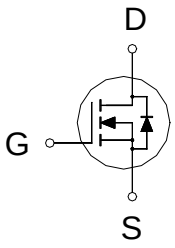
N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	40V
$R_{DSON\ (MAX.)}$	4mΩ
I_D	80A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current	T_C = 25 °C	I_D	80	A
	T_C = 100 °C		48	
Pulsed Drain Current[1]		I_{DM}	160	
Avalanche Current		I_{AS}	80	
Avalanche Energy	L = 0.1mH, ID=80A, RG=25Ω	E_{AS}	320	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	E_{AR}	160	
Power Dissipation	T_C = 25 °C	P_D	50	W
	T_C = 100 °C		20	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

100% UIS testing in condition of V_D=20V, L=0.1mH, V_G=10V, I_L=50A, Rated V_{DS}=40V N-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		2.5	°C / W
Junction-to-Ambient	$R_{\theta JA}$		50	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

[3]50°C / W when mounted on a 1 in^2 pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	40			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	2	3	4	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±30V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 32V, V_{GS} = 0V			1	μA
		V_{DS} = 30V, V_{GS} = 0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	80			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 24A		3.5	4.0	mΩ
		V_{GS} = 7V, I_D = 24A		5.2	6.5	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 24A		35		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		3970		pF
Output Capacitance	C_{oss}			650		
Reverse Transfer Capacitance	C_{rss}			597		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz		1.7		Ω
Total Gate Charge[1,2]	Q_g	V_{DS} = 20V, V_{GS} = 10V, I_D = 20A		83.6		nC
Gate-Source Charge[1,2]	Q_{gs}			18.7		
Gate-Drain Charge[1,2]	Q_{gd}			34.5		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = 20V, I_D = 20A, V_{GS} = 10V, R_{GS} = 6Ω		50		nS
Rise Time[1,2]	t_r			120		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			75		
Fall Time[1,2]	t_f			150		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				80	A
Pulsed Current[3]	I_{SM}				160	
Forward Voltage[1]	V_{SD}	I_F = 24A, V_{GS} = 0V			1.3	V
Reverse Recovery Time	t_{rr}	I_F = 24A, dI_F/dt = 100A / μS		30		nS
Reverse Recovery Charge	Q_{rr}			200		nC

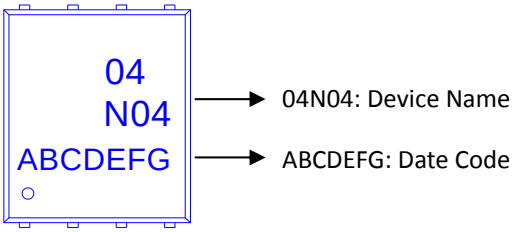
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

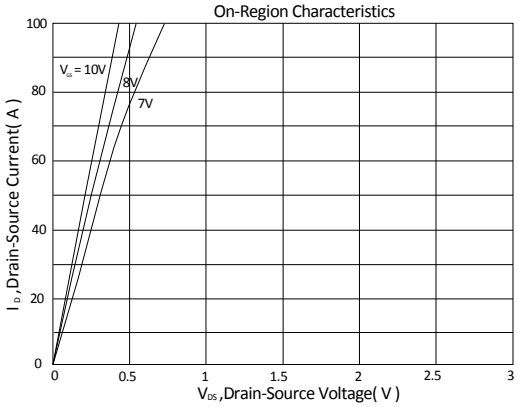
Ordering & Marking Information:

Device Name: LB04N04C for EDFN 5 x 6

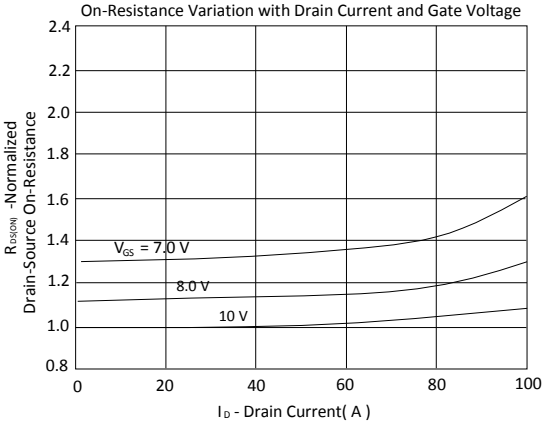


TYPICAL CHARACTERISTICS

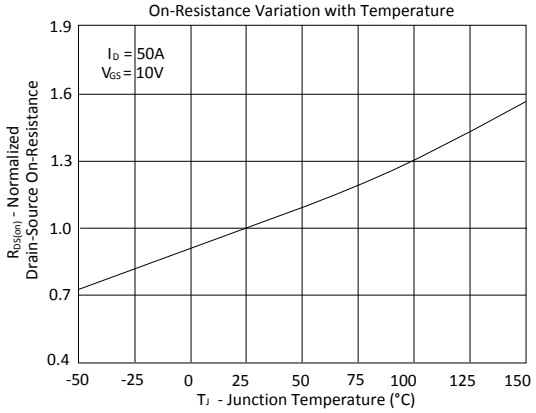
On-Region Characteristics



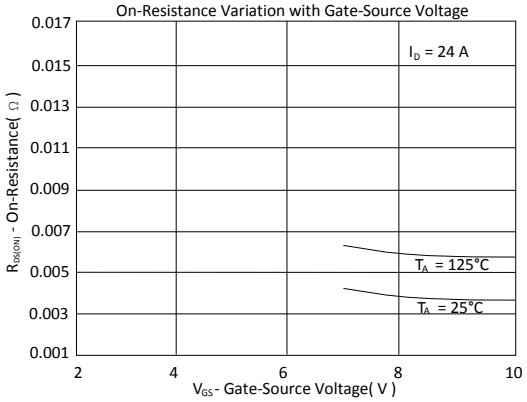
On-Resistance Variation with Drain Current and Gate Voltage



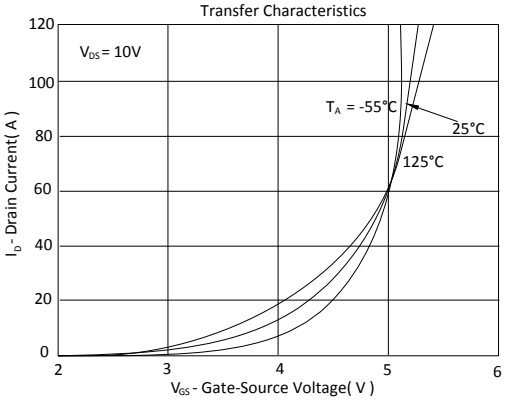
On-Resistance Variation with Temperature



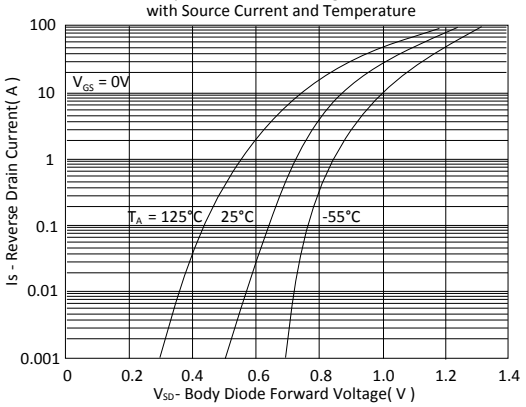
On-Resistance Variation with Gate-Source Voltage

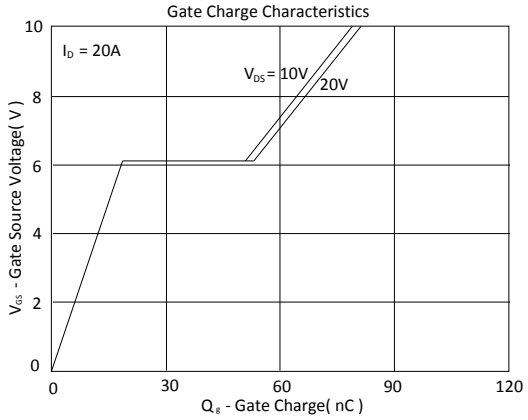


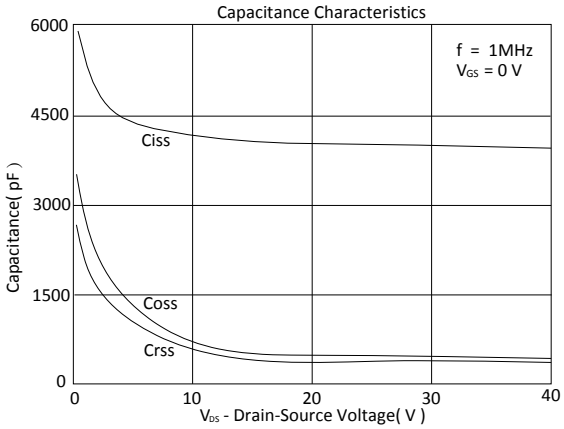
Transfer Characteristics

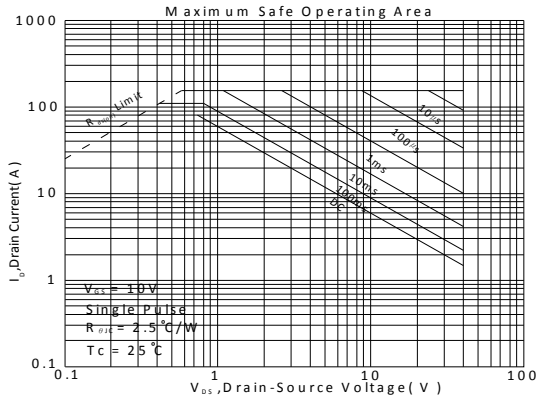


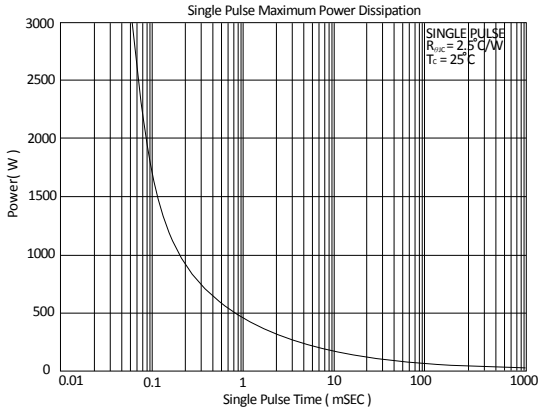
Body Diode Forward Voltage Variation
with Source Current and Temperature

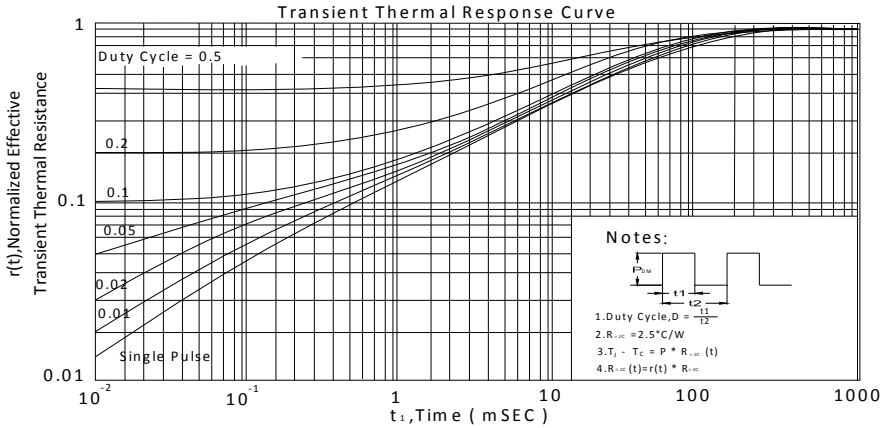



Gate Charge Characteristics
I_D = 20A
V_{DS}= 10V
20V
V_{GS} - Gate Source Voltage(V)
Q_g - Gate Charge(nC)

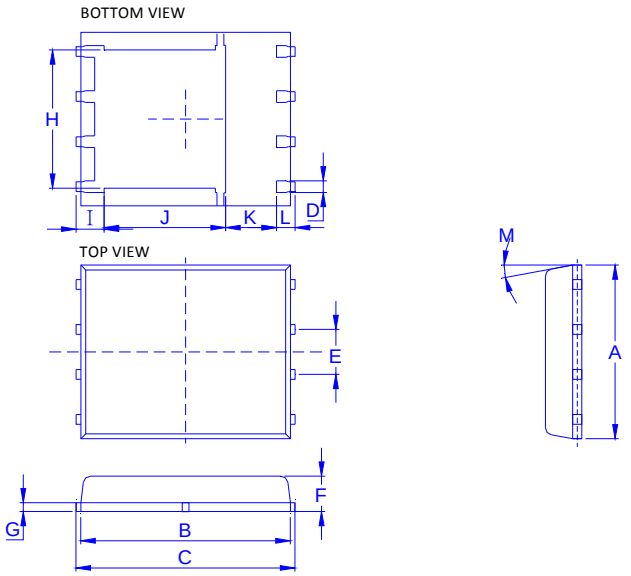

Capacitance Characteristics
f = 1MHz
V_{GS} = 0 V
Ciss
Coss
Crss
Capacitance(pF)
V_{DS} - Drain-Source Voltage(V)


Maximum Safe Operating Area
V_{GS} = 10V
Single Pulse
$R_{\theta JC}$ = 2.5°C/W
Tc = 25°C
I_D,Drain Current(A)
V_{DS},Drain-Source Voltage(V)


Single Pulse Maximum Power Dissipation
SINGLE PULSE
$R_{\theta JC}$ = 2.5°C/W
Tc = 25°C
Power(W)
Single Pulse Time (mSEC)


Transient Thermal Response Curve
Duty Cycle = 0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
Notes:
1.Duty Cycle,D = t1/t2
2.$R_{\theta JC}$ =2.5°C/W
3.T_J - T_C = P * $R_{\theta JC}$ (t)
4.$R_{\theta JC}$(t)=r(t) * $R_{\theta JC}$
r(t),Normalized Effective Transient Thermal Resistance
t_1,Time (mSEC)

Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K	L	M
Min.	4.80	5.50	5.90	0.3		0.85	0.15	3.67	0.41	3.00	0.94	0.45	0°
Typ.					1.27								
Max.	5.30	5.90	6.15	0.51		1.20	0.30	4.54	0.85	3.92	1.7	0.71	12°

Recommended minimum pads