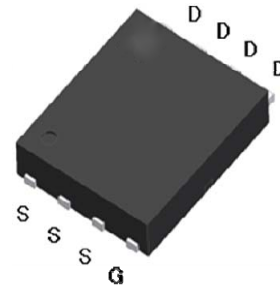
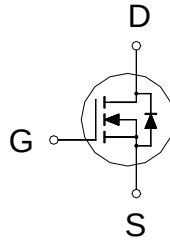


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	30V
R _{DS(on)} (MAX.)	1.7mΩ
I _D	100A



UIS, R_g 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current ¹	T _C = 25 °C	I _D	100	A
	T _C = 100 °C		100	
Pulsed Drain Current ²		I _{DM}	400	
Avalanche Current		I _{AS}	80	mJ
Avalanche Energy	L = 0.1mH, I _D =80A, R _G =25 Ω	E _{AS}	320	
Repetitive Avalanche Energy ³	L = 0.05mH	E _{AR}	160	
Power Dissipation	T _C = 25 °C	P _D	83	W
	T _C = 100 °C		33	
Operating Junction & Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C

100% UIS testing in condition of V_D=15V, L=0.1mH, V_G=10V, I_L=40A, Rated V_{DS}=30V N-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}		1.5	°C / W
Junction-to-Ambient ⁴	R _{θJA}		50	

¹Package Limited.

²Pulse width limited by maximum junction temperature.

³Duty cycle ≤ 1%

⁴50°C / W when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1	2	3	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 24V, V _{GS} = 0V			1	μA
		V _{DS} = 20V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	100			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 10V, I _D = 30A		1.4	1.7	mΩ
		V _{GS} = 4.5V, I _D = 30A		1.9	2.6	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 30A		50		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		6140		pF
Output Capacitance	C _{oss}			933		
Reverse Transfer Capacitance	C _{rss}			371		
Gate Resistance	R _g	V _{GS} = 15mV, V _{DS} = 0V, f = 1MHz		2.0		Ω
Total Gate Charge ^{1,2}	Q _g (V _{GS} =10V)	V _{DS} = 15V, V _{GS} = 10V, I _D = 30A		67		nC
	Q _g (V _{GS} =4.5V)			32		
Gate-Source Charge ^{1,2}	Q _{gs}			15		
Gate-Drain Charge ^{1,2}	Q _{gd}			14		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{DS} = 15V, I _D = 1A, V _{GS} = 10V, R _{GS} = 2.7Ω		20		nS
Rise Time ^{1,2}	t _r			15		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			60		
Fall Time ^{1,2}	t _f			30		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _c = 25 °C)						
Continuous Current ⁴	I _S				100	A
Pulsed Current ³	I _{SM}				400	
Forward Voltage ¹	V _{SD}	I _F = 30A, V _{GS} = 0V			1.2	V
Reverse Recovery Time	t _{rr}	I _F = I _S , dI _F /dt = 100A / μS		36		nS
Peak Reverse Recovery Current	I _{RM(REC)}			200		A
Reverse Recovery Charge	Q _{rr}			30		nC

¹Pulse test : Pulse Width $\leq 300\mu$ sec, Duty Cycle $\leq 2\%$.

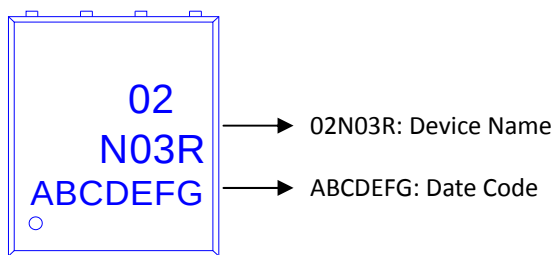
²Independent of operating temperature.

³Pulse width limited by maximum junction

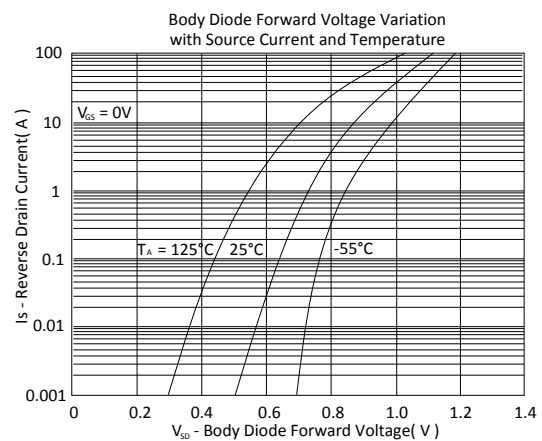
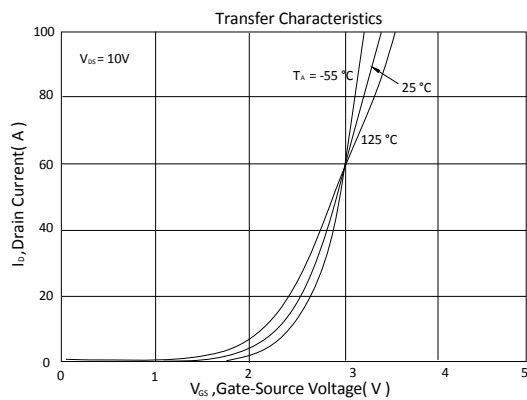
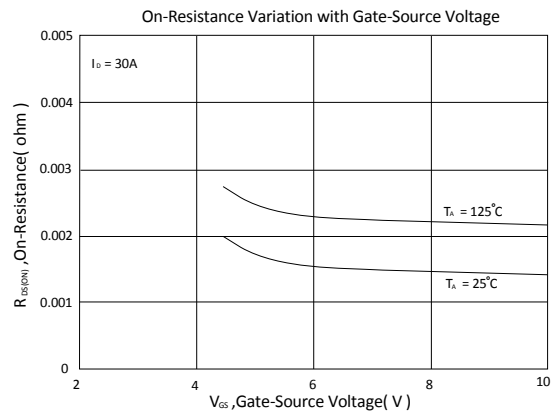
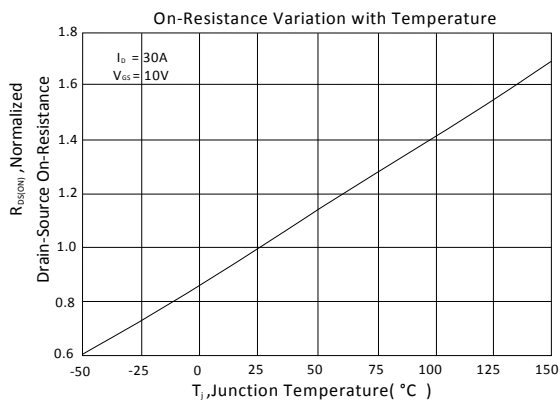
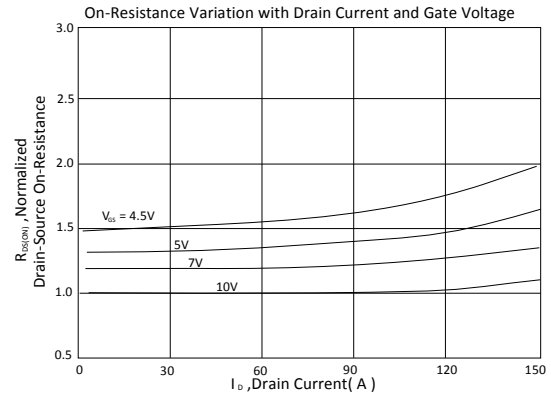
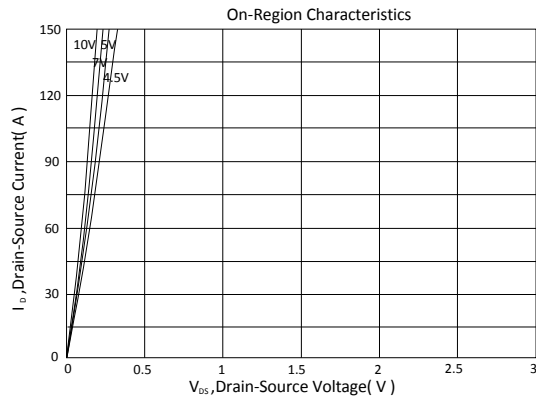
temperature. ⁴Package Limited.

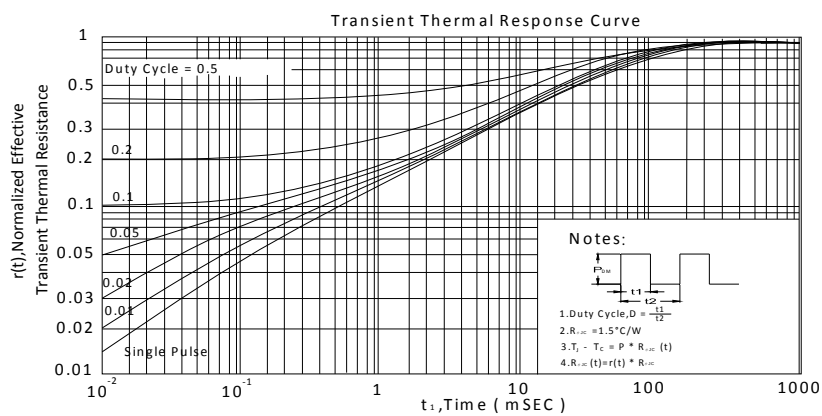
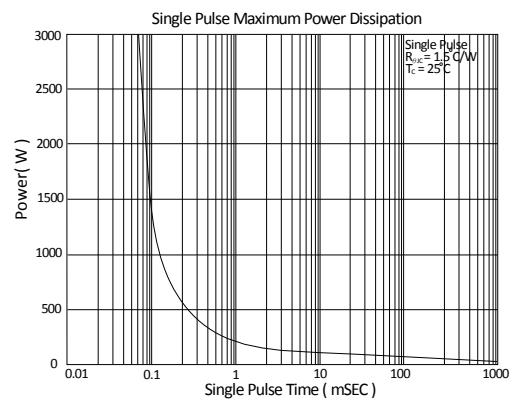
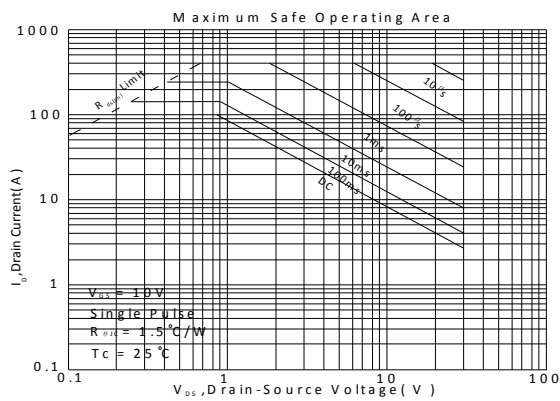
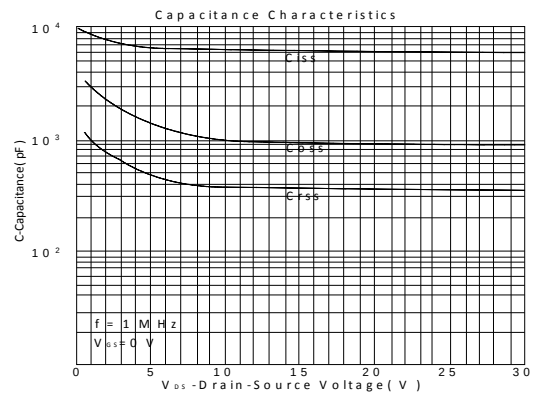
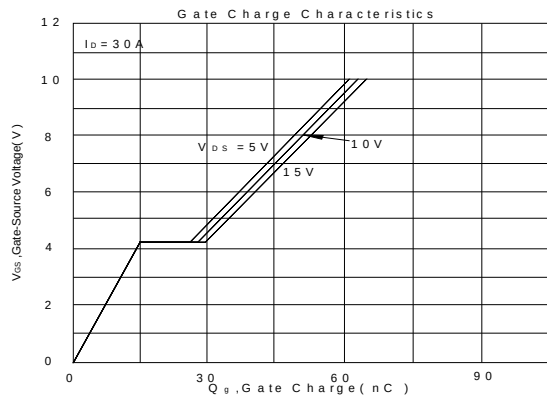
Ordering & Marking Information:

Device Name: LB02N03C for EDFN 5 x 6

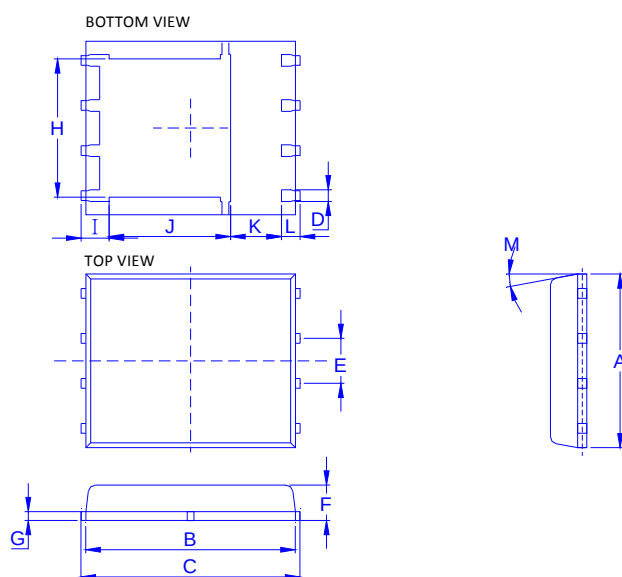


TYPICAL CHARACTERISTICS





Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K	L	M
Min.	4.80	5.50	5.90	0.3		0.85	0.15	3.67	0.41	3.00	0.94	0.45	0°
Typ.					1.27								
Max.	5.30	5.90	6.15	0.51		1.20	0.30	4.54	0.85	3.92	1.7	0.71	12°

Recommended minimum pads

