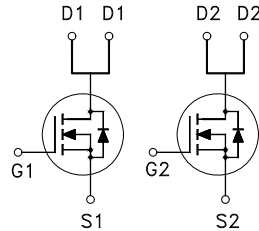


Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	250V
R _{DS(on)} (MAX.)	1.7 Ω
I _D	0.5A



R_g 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _A = 25 °C	I _D	0.5	A
	T _A = 100 °C		0.3	
Pulsed Drain Current ¹		I _{DM}	2	
Power Dissipation	T _A = 25 °C	P _D	2	W
	T _A = 70 °C		1.3	
Operating Junction & Storage Temperature Range		T _j , T _{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}		25	°C / W
Junction-to-Ambient ³	R _{θJA}		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

³62.5°C / W when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_c = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	250			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.0	2.0	3.0	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 200V, V _{GS} = 0V			1	μA
		V _{DS} = 200V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	0.5			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 10V, I _D = 0.25A		1.35	1.7	mΩ
		V _{GS} = 5V, I _D = 0.15A		1.5	2.0	
Forward Transconductance ¹	g _{fs}	V _{DS} = 50V, I _D = 0.25A		2.0		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 25V, f = 1MHz		680		pF
Output Capacitance	C _{oss}			15		
Reverse Transfer Capacitance	C _{rss}			13		
Gate Resistance	R _g	V _{GS} = 15mV, V _{DS} = 0V, f = 1MHz		3.0		Ω
Total Gate Charge ^{1,2}	Q _g	V _{DS} = 200V, V _{GS} = 10V, I _D = 0.25A		17.8		nC
Gate-Source Charge ^{1,2}	Q _{gs}			2.2		
Gate-Drain Charge ^{1,2}	Q _{gd}			4.4		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{DS} = 125V, I _D = 0.1A, V _{GS} = 10V, R _G = 6Ω		10		nS
Rise Time ^{1,2}	t _r			40		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			12		
Fall Time ^{1,2}	t _f			20		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _C = 25 °C)						
Continuous Current	I _S				0.5	A
Pulsed Current ³	I _{SM}				2	
Forward Voltage ¹	V _{SD}	I _F = I _S , V _{GS} = 0V			1.3	V

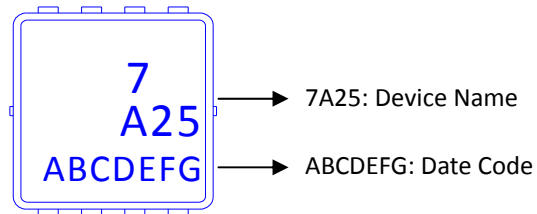
¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

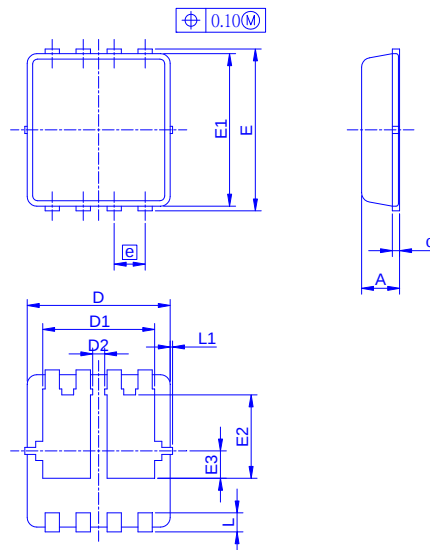
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: LBJ7N25BD for EDFN 3 x 3



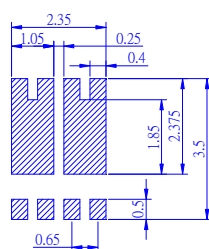
Outline Drawing



Dimension in mm

Dimension	A	A1	b	c	D	D1	D2	E	E1	E2	E3	e	L	L1	θ1
Min.	0.70	0	0.24	0.10	2.95	2.25		3.15	2.95	1.65			0.30	0	0°
Typ.	0.80		0.30	0.152	3.00	2.35	0.225	3.20	3.00	1.75	0.575	0.65	0.40		10°
Max.	0.90	0.05	0.35	0.25	3.05	2.45		3.25	3.05	1.85			0.50	0.10	12°

Recommended minimum pads



TYPICAL CHARACTERISTICS

