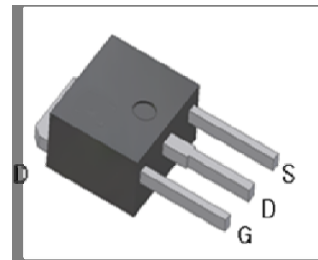
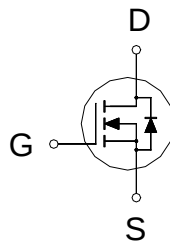


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	100V
R _{DS(on)} (MAX.)	150mΩ
I _D	10A



UIS, R_g 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _C = 25 °C	I _D	10	A
	T _C = 100 °C		7	
Pulsed Drain Current ¹		I _{DM}	40	
Avalanche Current		I _{AS}	12	mJ
Avalanche Energy	L = 0.1mH, I _D =12A, R _G =25Ω	E _{AS}	7.2	
Repetitive Avalanche Energy ²	L = 0.05mH	E _{AR}	3.6	
Power Dissipation	T _C = 25 °C	P _D	30	W
	T _C = 100 °C		13	
Operating Junction & Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}		4.2	°C / W
Junction-to-Ambient	R _{θJA}		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS ($T_c = 25\text{ }^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	100			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.0	2.0	3.0	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80V, V _{GS} = 0V			1	μA
		V _{DS} = 70V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	10			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 10V, I _D = 10A		130	150	mΩ
		V _{GS} = 5V, I _D = 10A		150	175	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 10A		8		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 25V, f = 1MHz		1030		pF
Output Capacitance	C _{oss}			50		
Reverse Transfer Capacitance	C _{rss}			42		
Gate Resistance	R _g	V _{GS} = 15mV, V _{DS} = 0V, f = 1MHz		1.2		Ω
Total Gate Charge ^{1,2}	Q _g	V _{DS} = 80V, V _{GS} = 10V, I _D = 10A		23		nC
Gate-Source Charge ^{1,2}	Q _{gs}			2.3		
Gate-Drain Charge ^{1,2}	Q _{gd}			6.1		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{DS} = 50V, I _D = 1A, V _{GS} = 10V, R _{GS} = 6Ω		12		nS
Rise Time ^{1,2}	t _r			20		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			25		
Fall Time ^{1,2}	t _f			25		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _c = 25 °C)						
Continuous Current	I _S				10	A
Pulsed Current ³	I _{SM}				40	
Forward Voltage ¹	V _{SD}	I _F = I _S , V _{GS} = 0V			1.3	V
Reverse Recovery Time	t _{rr}	I _F = 10A, dI _F /dt = 100A / μS		35		nS
Reverse Recovery Charge	Q _{rr}			65		nC

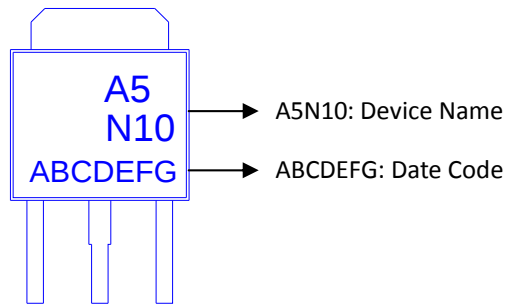
¹Pulse test : Pulse Width $\leq 300\text{ }\mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

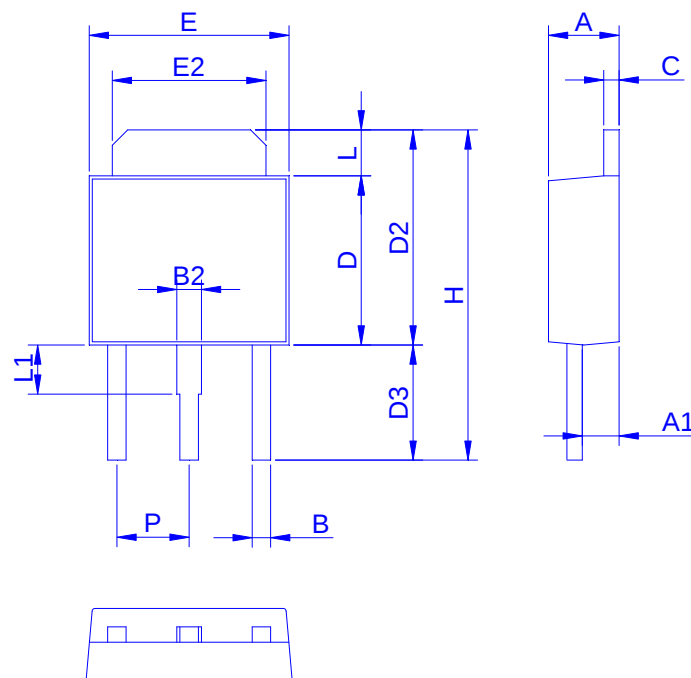
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: LBA5N10E for IPAK (TO-251)



Outline Drawing



Dimension in mm

Dimension	A	A1	B	B2	C	D	D2	D3	E	E2	H	L	L1	P
Min.	2.10	0.90	0.40	0.60	0.40	5.30	6.70	3.40	6.30	4.80	10.2	0.89	0.90	2.10
Max.	2.50	1.50	0.90	1.15	0.60	6.25	7.30	4.30	6.80	5.50	11.5	1.40	1.80	2.50

TYPICAL CHARACTERISTICS

