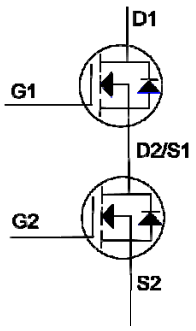
N-Channel Logic Level Enhancement Mode Field Effect Transistor

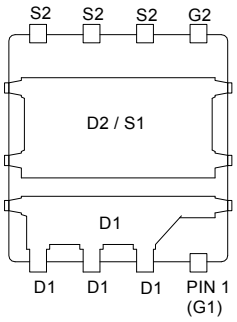
Product Summary:

	N-CH-Q1	N-CH-Q2
BV_{DSS}	40V	40V
$R_{DSON\ (MAX.)}$	17mΩ	8mΩ
I_D	41A	57A

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free





GREEN PRODUCT

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS Q1	LIMITS Q2	UNIT
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	41	57	A
	T_C = 100 °C		32	45	
Continuous Drain Current	T_A = 25 °C	I_D	9	12	
	T_A = 70 °C		7	9.6	
Pulsed Drain Current[1]		I_{DM}	84	114	
Avalanche Current		I_{AS}	30	40	
Avalanche Energy	L = 0.1mH, R_G=25Ω	E_{AS}	45	80	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	E_{AR}	22.5	40	
Power Dissipation	T_C = 25 °C	P_D	48	69	W
	T_C = 100 °C		19	27	
Power Dissipation	T_A = 25 °C	P_D	2.01	2.08	W
	T_A = 70 °C		1.2	1.3	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL		TYPICAL	MAXIMUM		UNIT
Junction-to-Case	$R_{\theta JC}$	Steady State		2.6	1.8	°C / W
Junction-to-Ambient[3]	$R_{\theta JA}$	Steady State		62	60	
	$R_{\theta JA}$	t ≦ 10 s		27	25	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

[3]$R_{\theta JA}$ when mounted on a 1 in^2 pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS			UNIT
				MIN	TYP	MAX	
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	Q1	40			V
			Q2	40			
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	Q1	1	1.7	3	
			Q2	1	1.7	3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	Q1			±100	nA
			Q2			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 32V, V_{GS} = 0V	Q1			1	μA
			Q2			1	
		V_{DS} = 30V, V_{GS} = 0V, T_J = 125 °C	Q1			25	
			Q2			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	Q1	41			A
			Q2	57			
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 6A	Q1		14	17	mΩ
		V_{GS} = 10V, I_D = 12A	Q2		6.2	8	
		V_{GS} = 4.5V, I_D = 4A	Q1		22	32	
		V_{GS} = 4.5V, I_D = 10A	Q2		7.8	12	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 6A	Q1		15		S
		V_{DS} = 5V, I_D = 12A	Q2		18		
DYNAMIC							
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 20V, f = 1MHz	Q1		707		pF
			Q2		1962		
Output Capacitance	C_{oss}		Q1		98		
			Q2		245		
Reverse Transfer Capacitance	C_{rss}		Q1		81		
			Q2		225		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz	Q1		1.5		Ω
			Q2		1.4		
Total Gate Charge[1,2]	Q_g(V_{GS}=10V)	Q1	Q1		18		

		V_{DD} = 20V, V_{GS} = 10V,	Q2		47		
	Q_g(V_{GS}=4.5V)	I_D = 6A	Q1		10		
		Q2	Q2		24		
Gate-Source Charge[1,2]	Q_{gs}	V_{DD} = 20V, V_{GS} = 10V, I_D = 12A	Q1		2.4		
			Q2		6.8		
Gate-Drain Charge[1,2]	Q_{gd}		Q1		6.0		
			Q2		16		
Turn-On Delay Time[1,2]	$t_{d(on)}$		Q1		6		nS
			Q2		10		
Rise Time[1,2]	t_r	V_{DD} = 20V,	Q1		10		
			Q2		18		
Turn-Off Delay Time[1,2]	$t_{d(off)}$	I_D = 1A, V_{GS} = 10V, R_{GS} = 2.7Ω	Q1		18		
			Q2		20		
Fall Time[1,2]	t_f		Q1		12		
			Q2		15		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)							
Continuous Current	I_S		Q1			41	A
			Q2			57	
Pulsed Current[3]	I_{SM}		Q1			84	
			Q2			114	
Forward Voltage[1]	V_{SD}	I_F = 6A, V_{GS} = 0V	Q1			1.3	V
		I_F = 12A, V_{GS} = 0V	Q2			1.3	
Reverse Recovery Time	t_{rr}	Q1	Q1		18		nS
		I_F = 6A, dI_F/dt = 100A / μS	Q2		22		
Reverse Recovery Charge	Q_{rr}	Q2	Q1		5		nC
		I_F = 12A, dI_F/dt = 100A / μS	Q2		6		

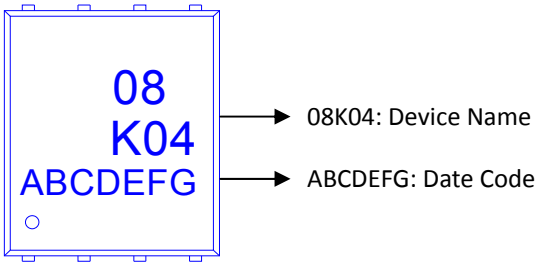
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

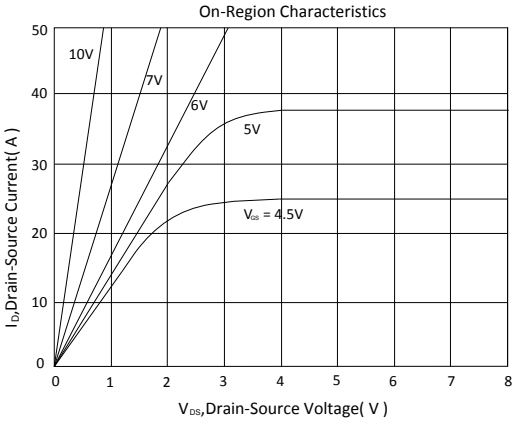
[3]Pulse width limited by maximum junction temperature.

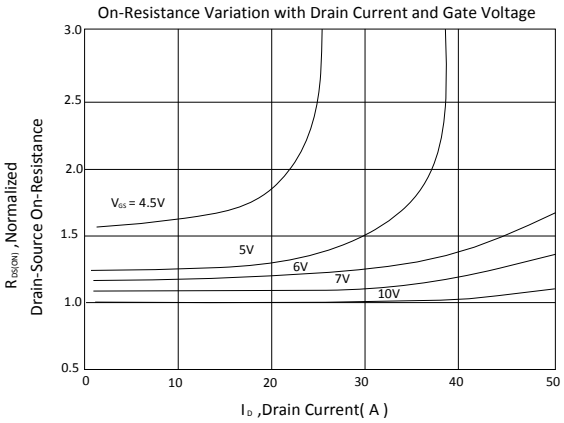
Ordering & Marking Information:

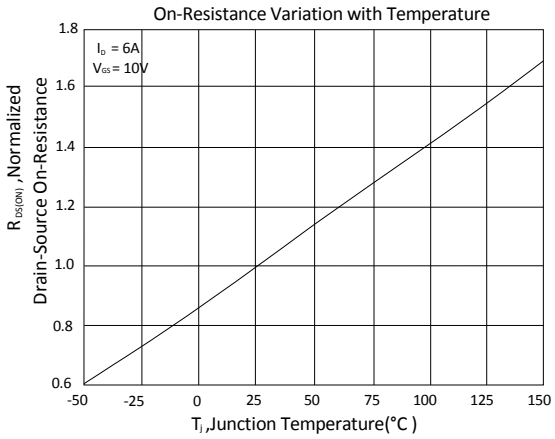
Device Name: LB7N25Q for Asymmetric Dual EDFN 5 x 6

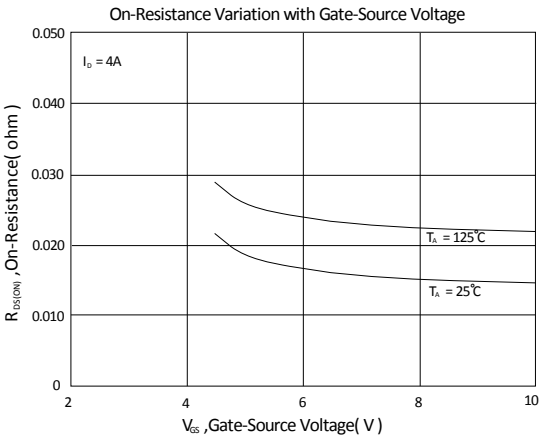


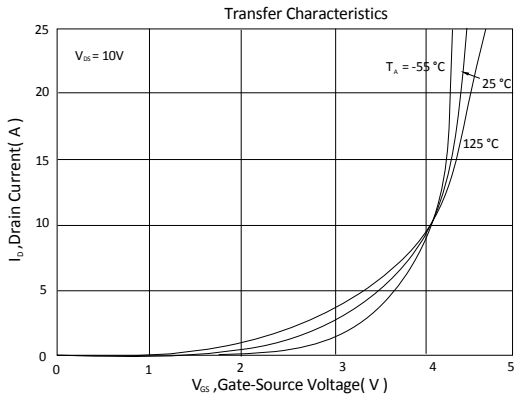
Q1 TYPICAL CHARACTERISTICS

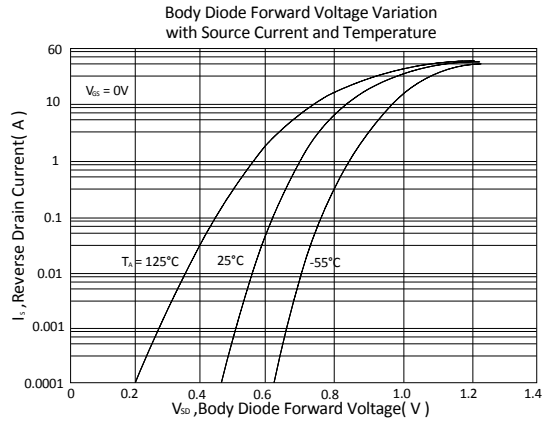


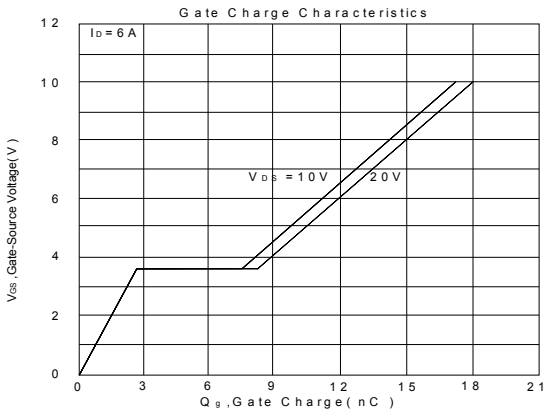


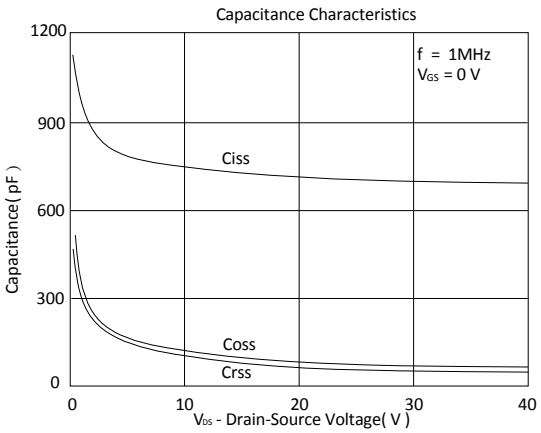


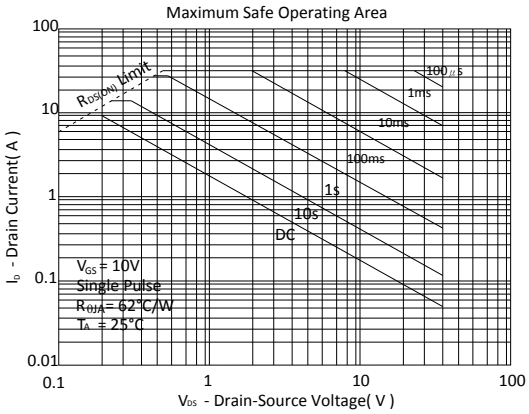


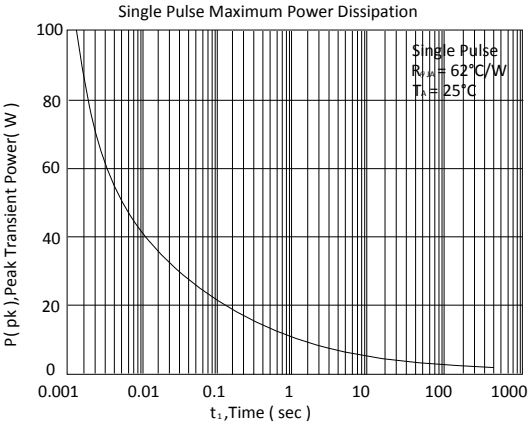


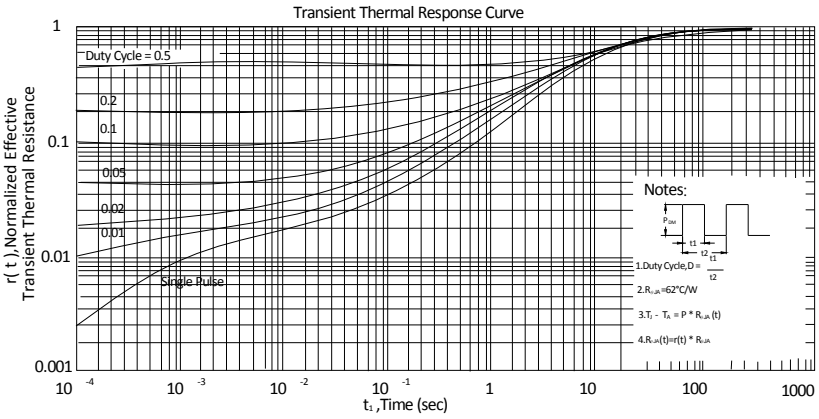



Gate Charge Characteristics
I D = 6 A
V DS = 10 V
20 V
VGS ,Gate-Source Voltage(V)
Q g ,Gate Charge(nC)

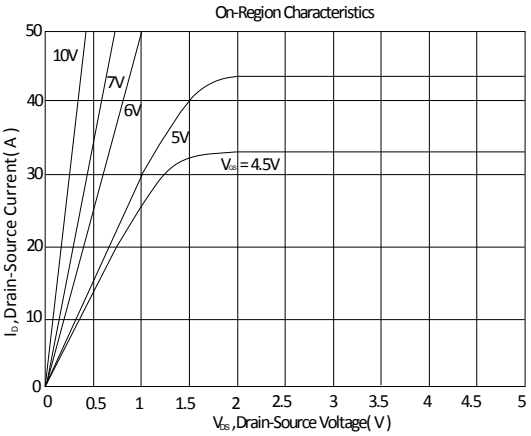

Capacitance Characteristics
f = 1MHz
VGS = 0 V
Ciss
Coss
Crss
Capacitance(pF)
VDS - Drain-Source Voltage(V)

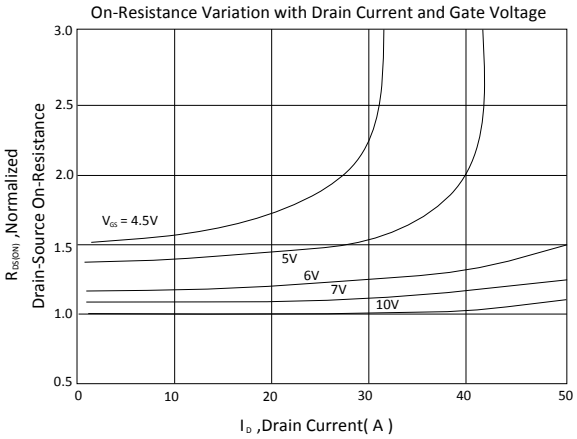

Maximum Safe Operating Area
RDS(ON) Limit
100 μs
1ms
10ms
100ms
1s
10s
DC
VGS = 10V
Single Pulse
RθJA= 62°C/W
TA = 25°C
ID - Drain Current(A)
VDS - Drain-Source Voltage(V)

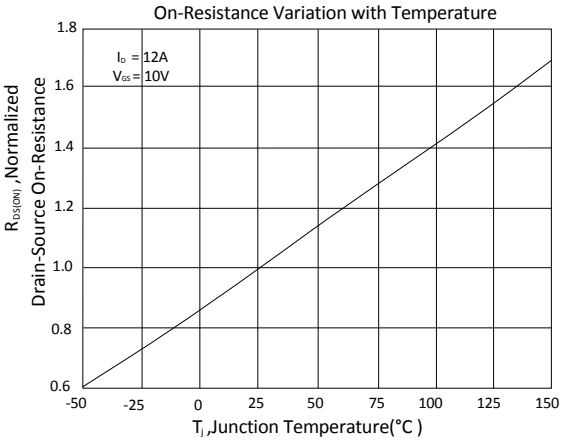

Single Pulse Maximum Power Dissipation
Single Pulse
RθJA = 62°C/W
TA = 25°C
P(pk),Peak Transient Power(W)
t1 ,Time (sec)

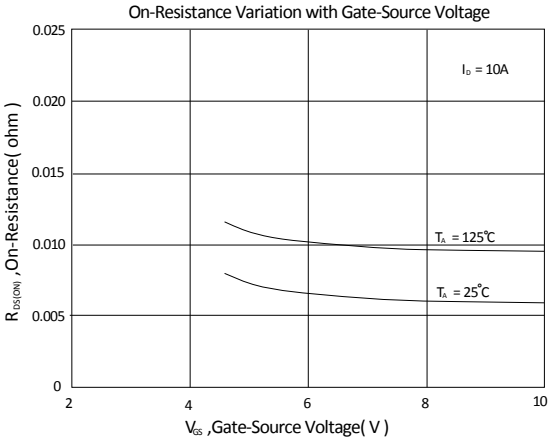

Transient Thermal Response Curve
Duty Cycle = 0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
Notes:
1.Duty Cycle,D =
2.RθJA=62°C/W
3.TJ - TA = P * RθJA (t)
4.RθJA(t)=r(t) * RθJA
r(t),Normalized Effective Transient Thermal Resistance
t1 ,Time (sec)

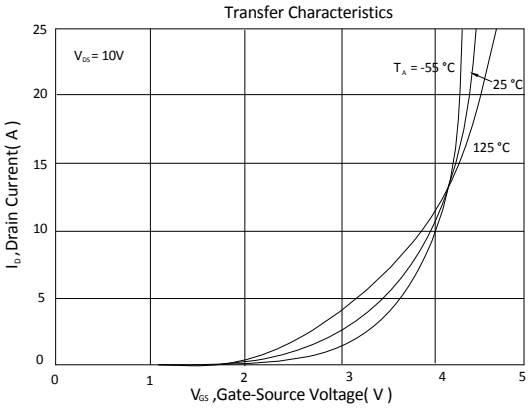
Q2 TYPICAL CHARACTERISTICS

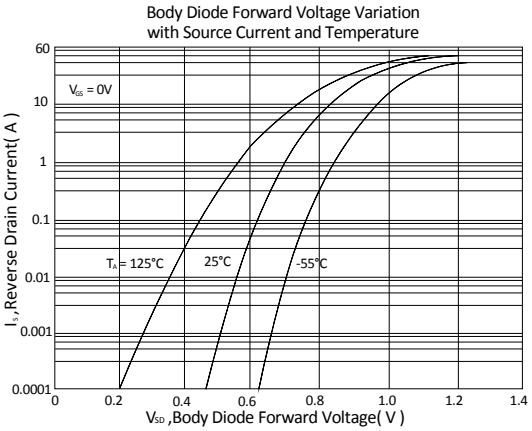


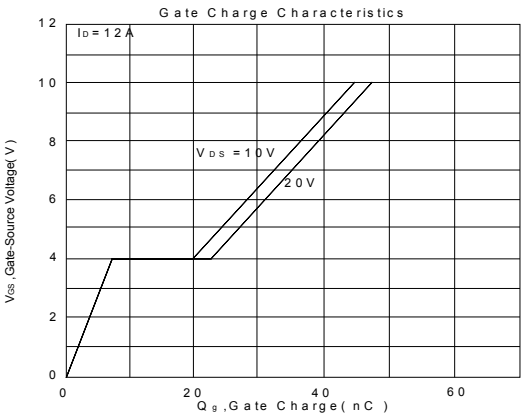


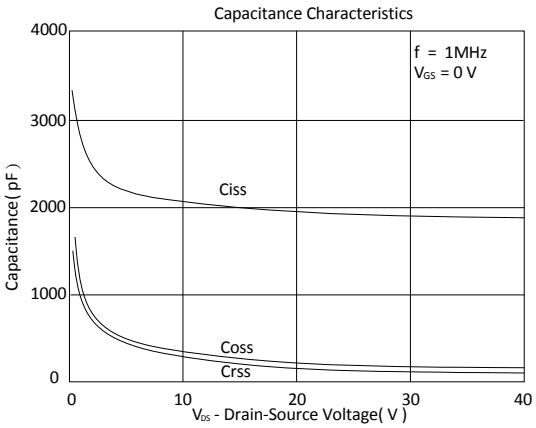









Gate Charge Characteristics
ID = 12A
VDS = 10V
20V
VGS ,Gate-Source Voltage(V)
Qg ,Gate Charge(nC)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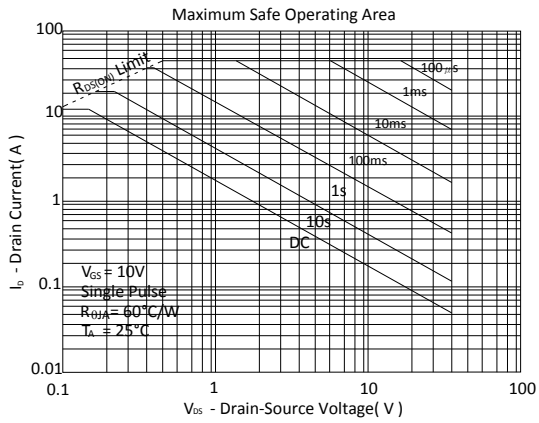
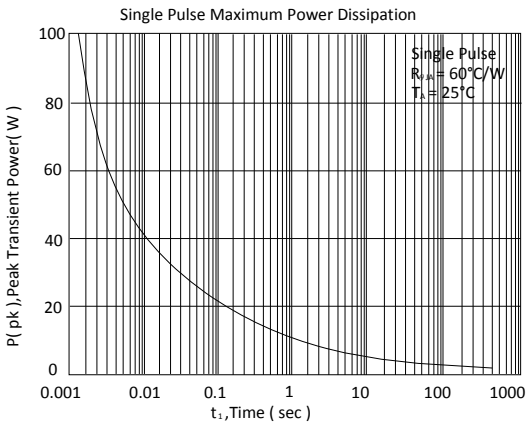
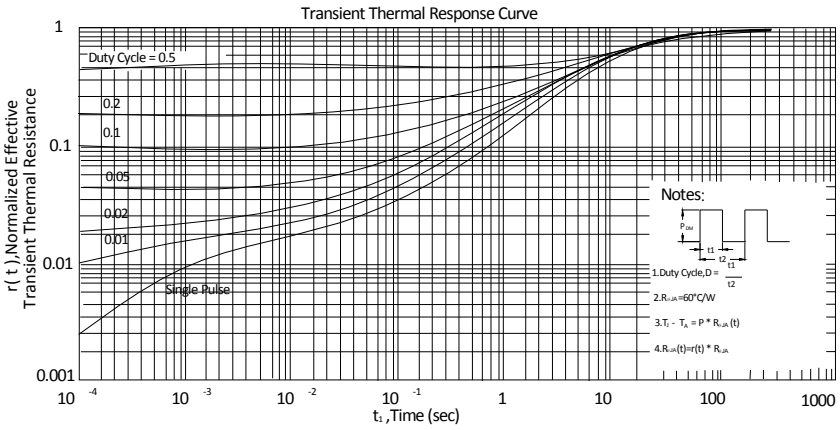
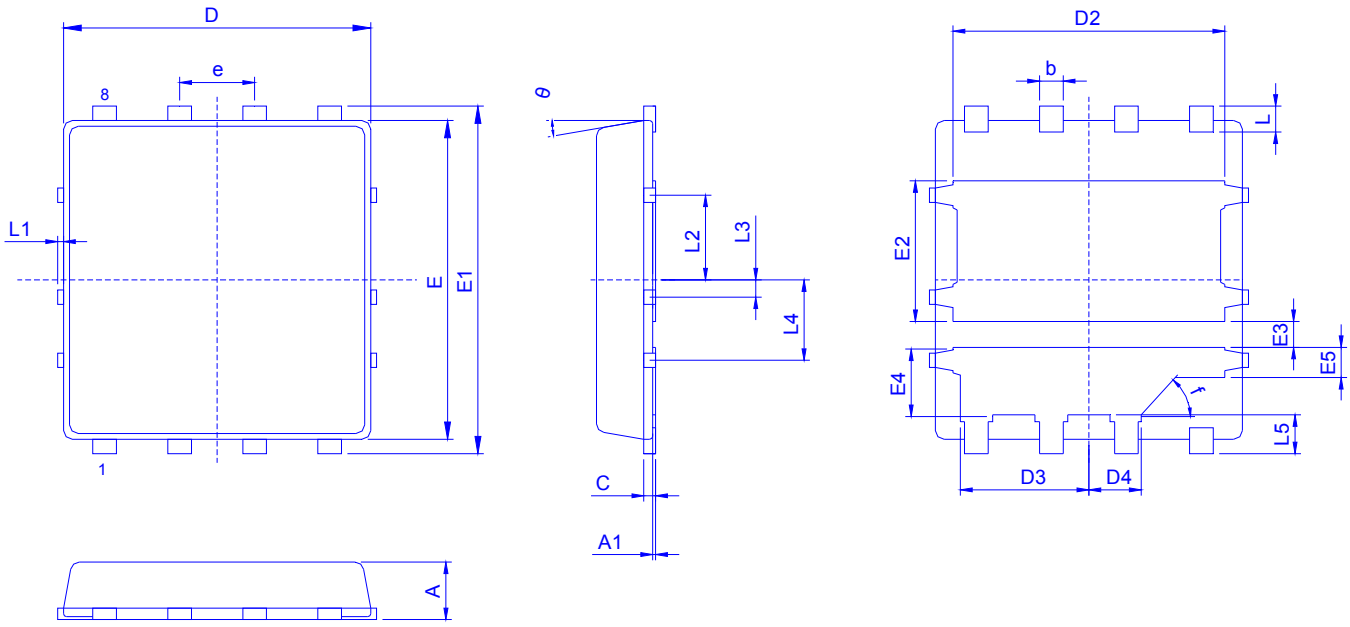

Maximum Safe Operating Area
RDS(on) Limit
100μs
1ms
10ms
100ms
1s
10s
DC
VGS = 10V
Single Pulse
RθJA= 60°C/W
TA = 25°C
ID - Drain Current(A)
VDS - Drain-Source Voltage(V)


Single Pulse Maximum Power Dissipation
Single Pulse
RθJA = 60°C/W
TA = 25°C
P(pk),Peak Transient Power(W)
t1 ,Time (sec)


Transient Thermal Response Curve
Duty Cycle = 0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
Notes:
1.Duty Cycle,D =
2.RθJA=60°C/W
3.TJ - TA = P * RθJA (t)
4.RθJA(t)=r(t) * RθJA
r(t),Normalized Effective Transient Thermal Resistance
t1 ,Time (sec)

Outline Drawing



Dimension in mm

Dimension	A	A1	b	c	D	D2	D3	D4	E	E1	E2	E3	E4	E5
Min.	0.85	0.00	0.35	0.15		4.5	2.125	0.835			2.4	0.40	1.125	0.475
Typ.	0.90		0.40	0.20	5.2	4.6	2.175	0.885	5.55	6.05	2.45	0.45	1.175	0.525
Max.	1.00	0.05	0.45	0.25		4.7	2.225	0.935			2.5	0.50	1.225	0.575

Dimension	e	L	L1	L2	L3	L4	L5	F	θ
Min.		0.35	0	1.375	0.2	1.3	0.575		0°
Typ.	1.27	0.45		1.475	0.3	1.4	0.675	45°	
Max.		0.55	0.1	1.575	0.4	1.5	0.775		10°

Recommended minimum pads