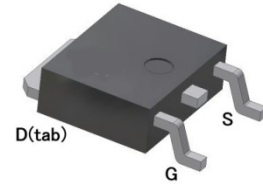


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	80V
R _{DS(on)} (MAX.)	65mΩ
I _D	15A



UIS, 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _C = 25 °C	I _D	15	A
	T _C = 100 °C		10	
Pulsed Drain Current ¹		I _{DM}	60	
Avalanche Current		I _{AS}	23	mJ
Avalanche Energy	L = 0.1mH, I _D =23A, R _G =25Ω	E _{AS}	27	
Repetitive Avalanche Energy ²	L = 0.05mH	E _{AR}	13	
Power Dissipation	T _C = 25 °C	P _D	39	W
	T _C = 100 °C		15	
Operating Junction & Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}		3.2	°C / W
Junction-to-Ambient ³	R _{θJA}		50	

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS ($T_c = 25\text{ }^{\circ}\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	80			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.0	1.7	3.0	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 64V, V_{GS} = 0V$			1	μA
		$V_{DS} = 60V, V_{GS} = 0V, T_J = 125\text{ }^{\circ}C$			25	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 5V, V_{GS} = 10V$	15			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 15A$		55	65	m Ω
		$V_{GS} = 5V, I_D = 10A$		68	85	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 15A$		12		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 30V, f = 1MHz$		1110		pF
Output Capacitance	C_{oss}			60		
Reverse Transfer Capacitance	C_{rss}			51		
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = 40V, V_{GS} = 10V,$ $I_D = 15A$		15		nC
Gate-Source Charge ^{1,2}	Q_{gs}			1.7		
Gate-Drain Charge ^{1,2}	Q_{gd}			4.1		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = 40V,$ $I_D = 1A, V_{GS} = 10V, R_{GS} = 6\Omega$		10		nS
Rise Time ^{1,2}	t_r			8		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			18		
Fall Time ^{1,2}	t_f			6		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_c = 25\text{ }^{\circ}C$)						
Continuous Current	I_S				15	A
Pulsed Current ³	I_{SM}				60	
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			1.3	V
Reverse Recovery Time	t_{rr}	$I_F = 10A, dI_F/dt = 100A / \mu S$		120		nS
Reverse Recovery Charge	Q_{rr}			500		nC

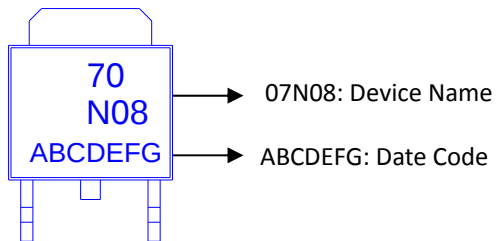
¹Pulse test : Pulse Width $\leq 300\text{ }\mu\text{sec}$, Duty Cycle $\leq 2\%$.

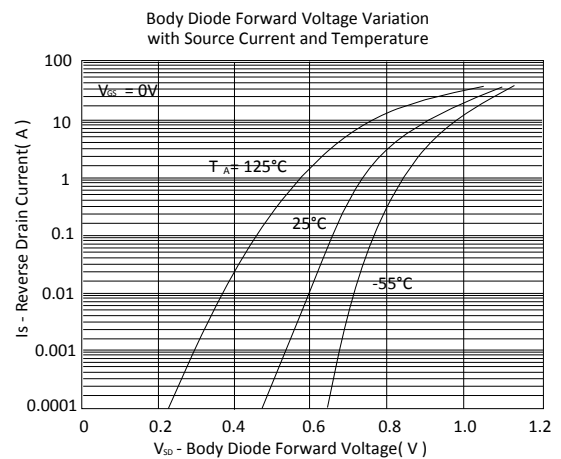
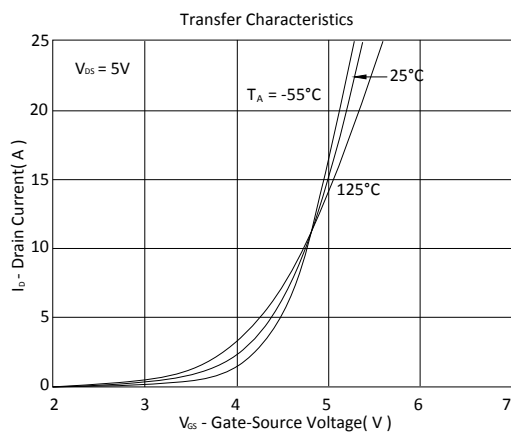
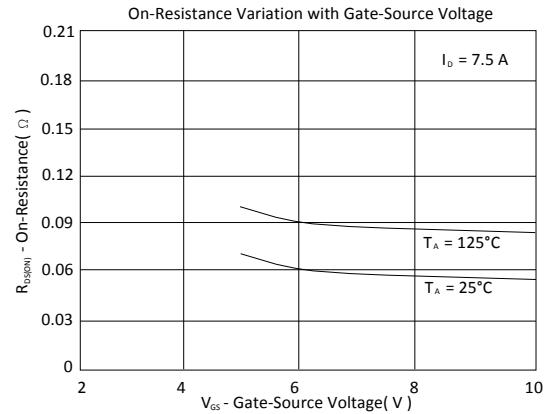
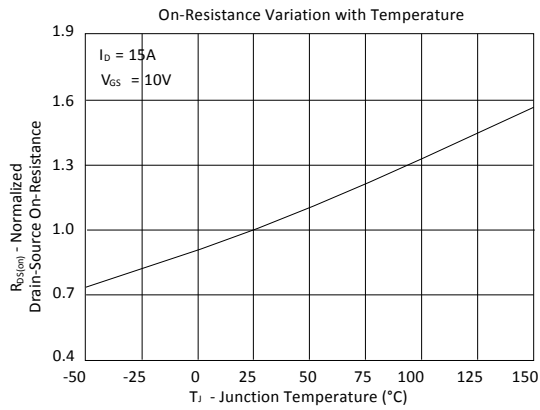
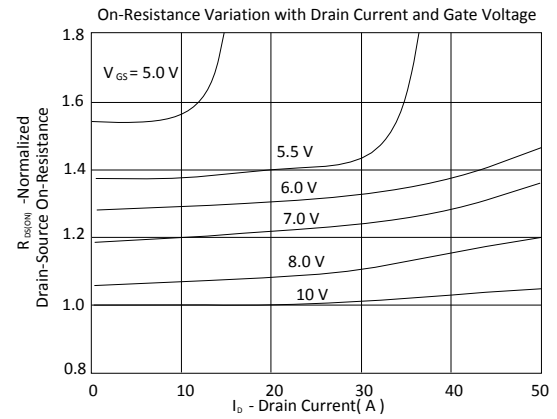
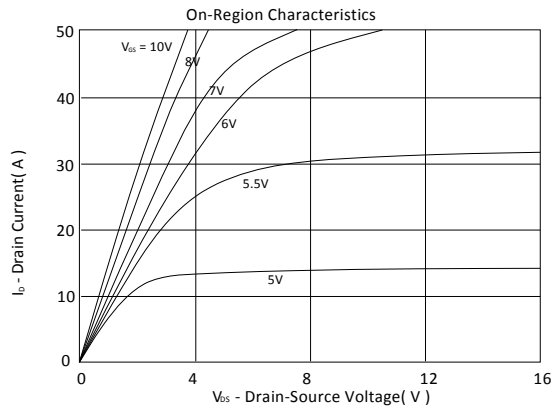
²Independent of operating temperature.

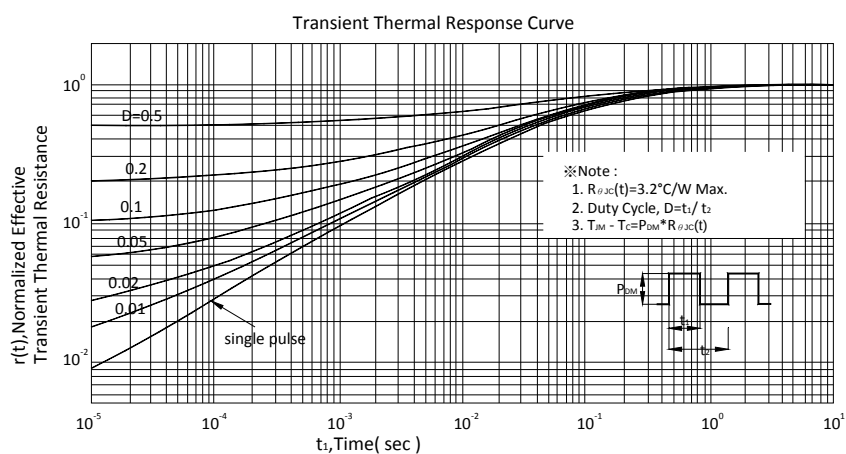
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

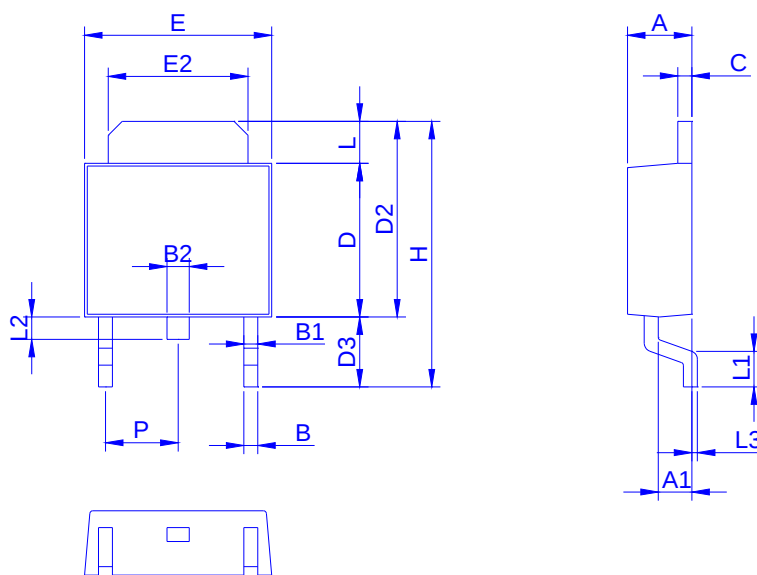
Device Name: LB70N08D for DPAK (TO-252)







Outline Drawing



Dimension in mm

Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	0.95	0.30	0.40	0.60	0.40	5.30	6.70	2.20	6.40	4.80	9.20	0.89	0.90	0.50	0.00	2.10
Max.	2.50	1.30	0.85	0.94	1.00	0.60	6.20	7.30	3.00	6.70	5.45	10.15	1.70	1.65	1.10	0.30	2.50

Footprint

