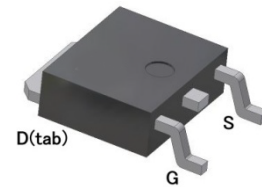
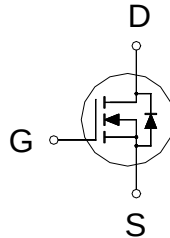


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	150V
$R_{DS(on)} (MAX.)$	50m Ω
I_D	36A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^{\circ}\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Drain-Source Voltage		V_{DSS}	150	V
Gate-Source Voltage		V_{GS}	± 30	V
Continuous Drain Current	$T_C = 25\text{ }^{\circ}\text{C}$	I_D	36	A
	$T_C = 100\text{ }^{\circ}\text{C}$		22	
Pulsed Drain Current ¹		I_{DM}	120	
Avalanche Current		I_{AS}	18	
Avalanche Energy	$L = 0.2\text{mH}$, $I_D = 18\text{A}$, $R_G = 25\Omega$	E_{AS}	32.4	mJ
Repetitive Avalanche Energy ²	$L = 0.1\text{mH}$	E_{AR}	16.2	
Power Dissipation	$T_C = 25\text{ }^{\circ}\text{C}$	P_D	104	W
	$T_C = 100\text{ }^{\circ}\text{C}$		41	
Operating Junction & Storage Temperature Range		$T_{j, T_{stg}}$	-55 to 150	$^{\circ}\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		1.2	$^{\circ}\text{C} / \text{W}$
Junction-to-Ambient ³	$R_{\theta JA}$		75	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³75 $^{\circ}\text{C} / \text{W}$ when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_c = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	150			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.5	2.5	4.0	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±30V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 120V, V _{GS} = 0V			1	μA
		V _{DS} = 100V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	48			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 10V, I _D = 20A		40	50	mΩ
		V _{GS} = 7V, I _D = 15A		48	60	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 20A		40		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 25V, f = 1MHz		4905		pF
Output Capacitance	C _{oss}			238		
Reverse Transfer Capacitance	C _{rss}			200		
Gate Resistance	R _g	V _{GS} = 15mV, V _{DS} = 0V, f = 1MHz		2.0		Ω
Total Gate Charge ^{1,2}	Q _g	V _{DS} = 80V, V _{GS} = 10V, I _D = 20A		67.5		nC
Gate-Source Charge ^{1,2}	Q _{gs}			12.7		
Gate-Drain Charge ^{1,2}	Q _{gd}			16.6		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{DS} = 75V, I _D = 1A, V _{GS} = 10V, R _{GS} = 6Ω		20		nS
Rise Time ^{1,2}	t _r			18		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			40		
Fall Time ^{1,2}	t _f			18		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _C = 25 °C)						
Continuous Current	I _S				36	A
Pulsed Current ³	I _{SM}				120	
Forward Voltage ¹	V _{SD}	I _F = I _S , V _{GS} = 0V			1.3	V
Reverse Recovery Time	t _{rr}	I _F = 25A, dI _F /dt = 100A / μS		120		nS
Reverse Recovery Charge	Q _{rr}			380		nC

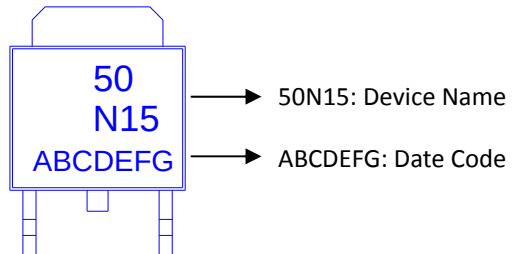
¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

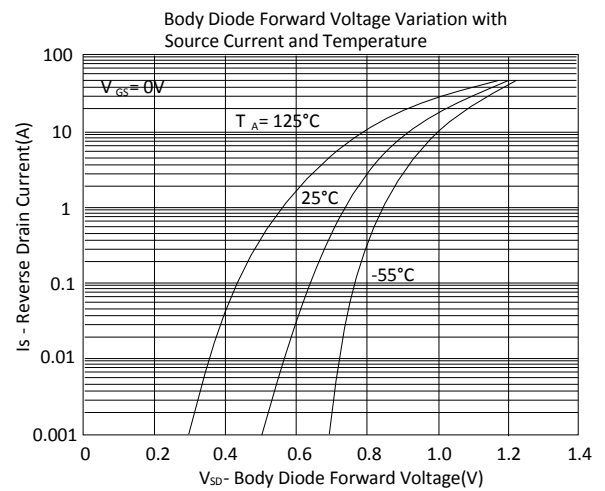
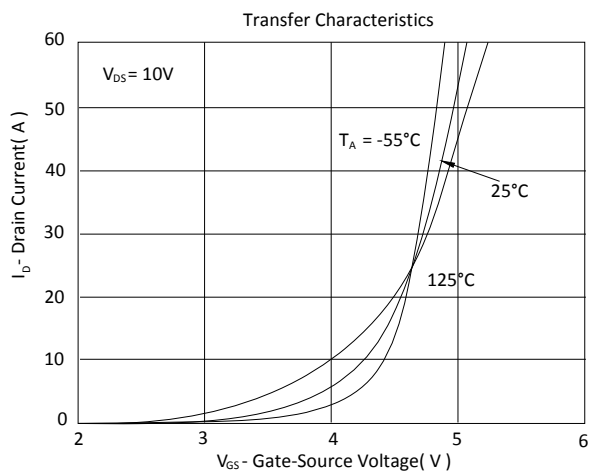
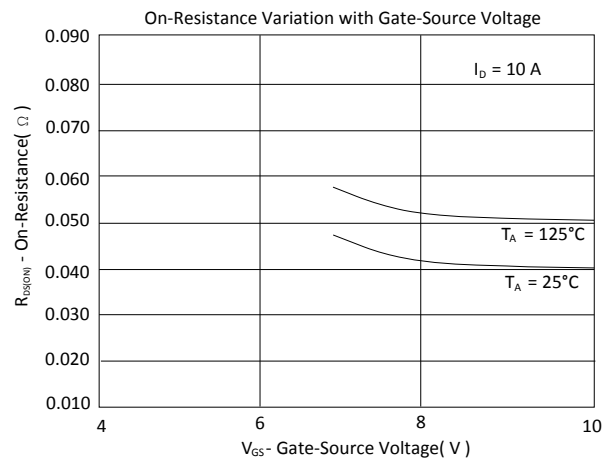
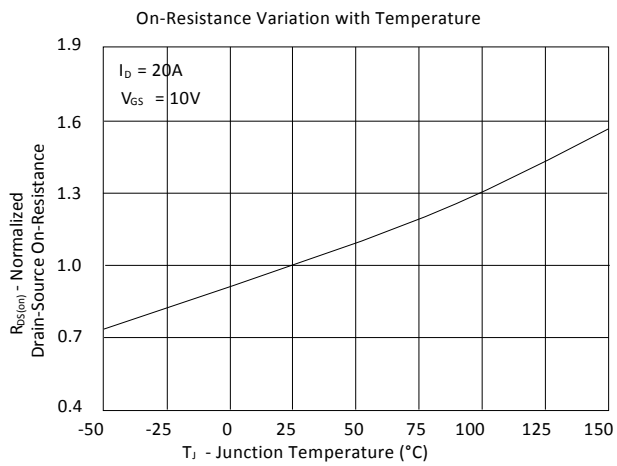
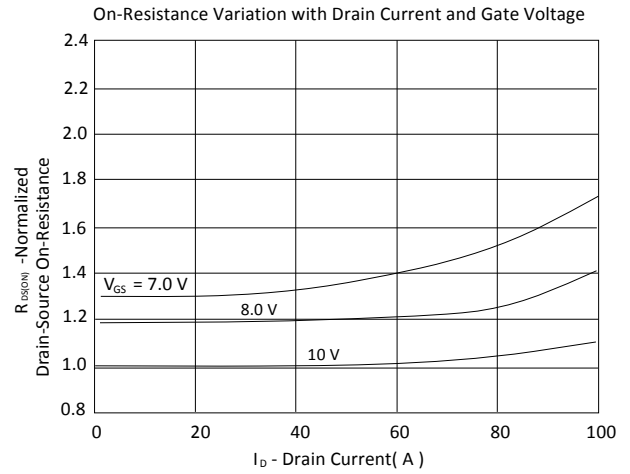
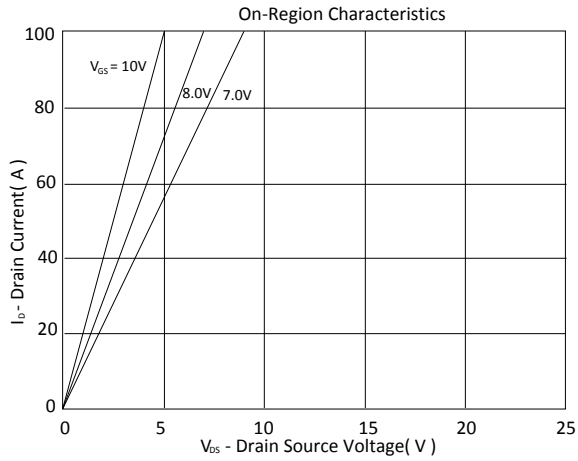
³Pulse width limited by maximum junction temperature.

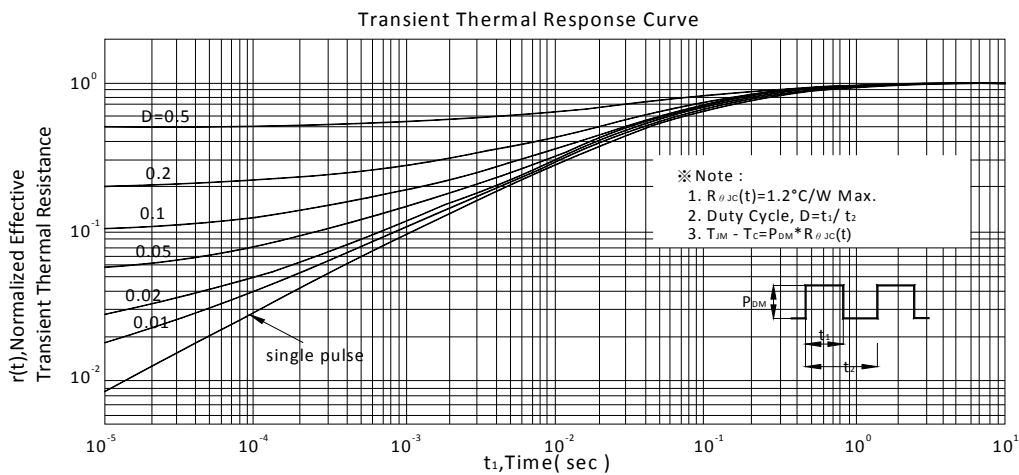
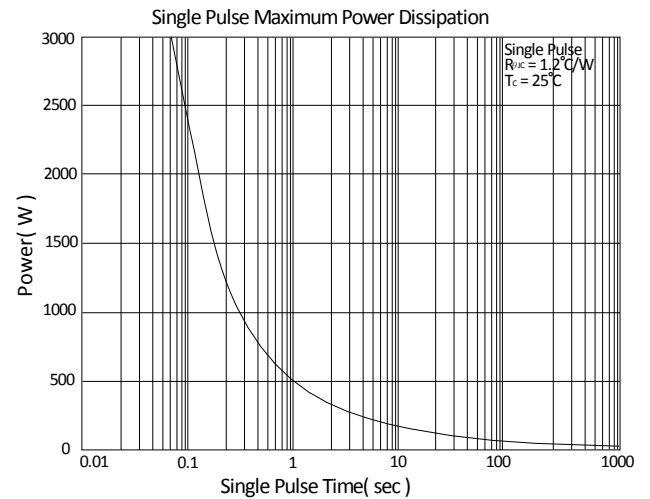
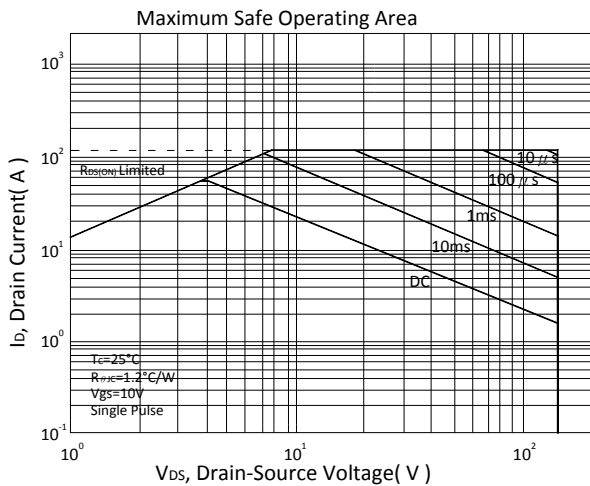
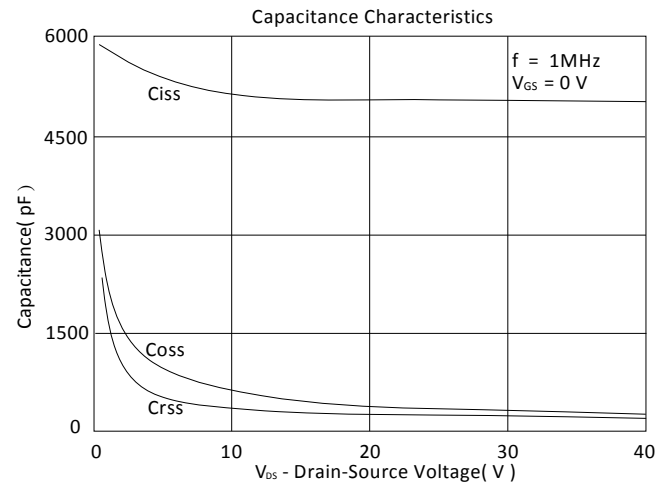
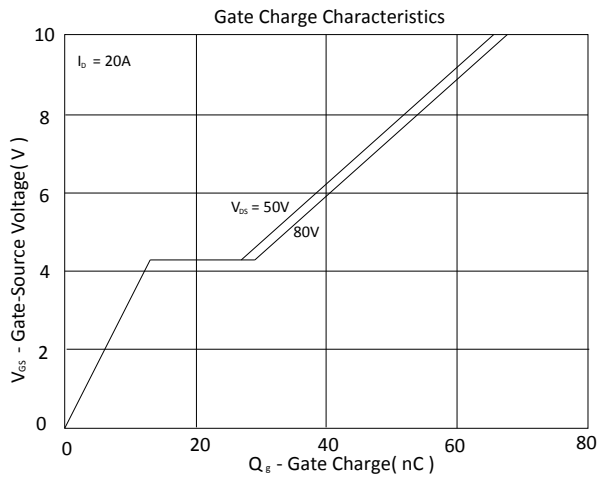
Ordering & Marking Information:

Device Name: LB50N15D for DPAK (TO-252)

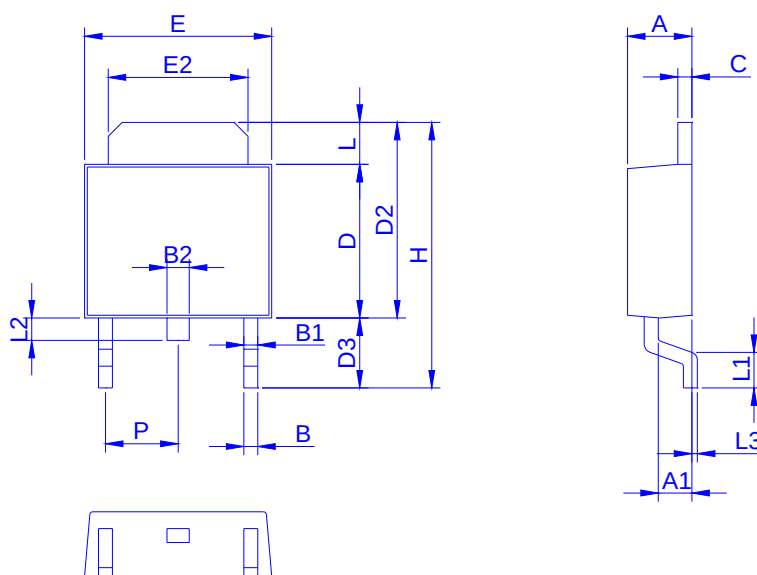


TYPICAL CHARACTERISTICS





Outline Drawing



Dimension in mm

Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	0.95	0.30	0.40	0.60	0.40	5.30	6.70	2.20	6.40	4.80	9.20	0.89	0.90	0.50	0.00	2.10
Max.	2.50	1.30	0.85	0.94	1.00	0.60	6.20	7.30	3.00	6.70	5.45	10.15	1.70	1.65	1.10	0.30	2.50

Footprint

