

N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	30V
$R_{DS(on)} (MAX.)$	50m Ω
I_D	3.5A



Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 12	V
Continuous Drain Current	$T_A = 25\text{ }^{\circ}\text{C}$	I_D	3.5	A
	$T_A = 70\text{ }^{\circ}\text{C}$		2.4	
Pulsed Drain Current ¹		I_{DM}	14	
Power Dissipation	$T_A = 25\text{ }^{\circ}\text{C}$	P_D	1.04	W
	$T_A = 70\text{ }^{\circ}\text{C}$		0.66	
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150	$^{\circ}\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Ambient ³	$R_{\theta JA} (T \leq 10\text{sec})$		83	$^{\circ}\text{C} / \text{W}$
	$R_{\theta JA} (\text{Steady State})$		120	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³The device mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$, Unless Otherwise Noted)

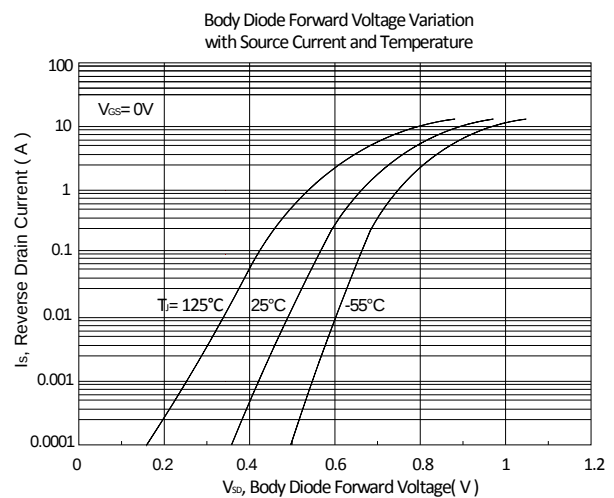
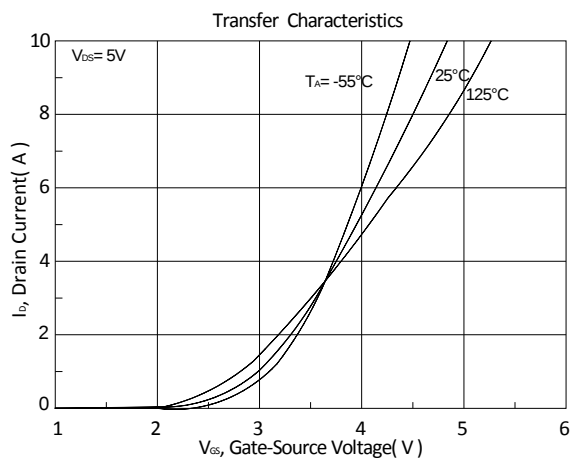
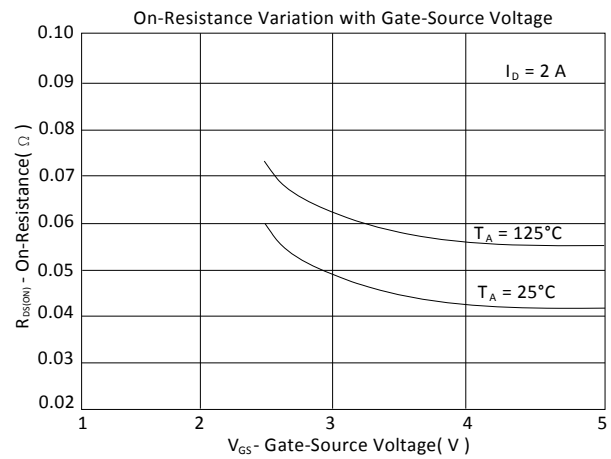
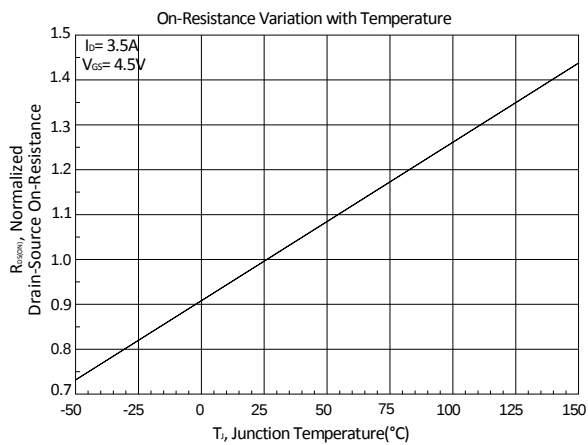
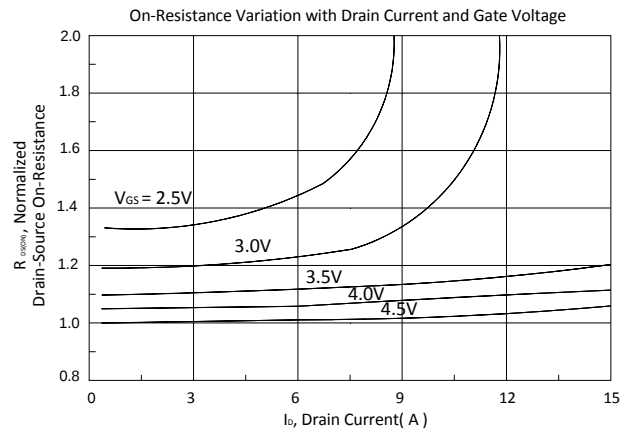
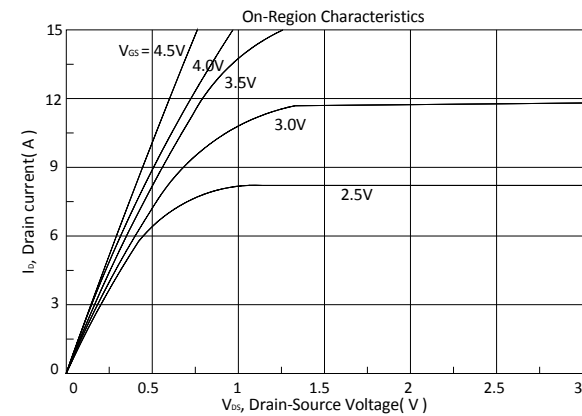
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.45	0.75	1.2	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24V, V_{GS} = 0V$			1	μA
		$V_{DS} = 20V, V_{GS} = 0V, T_J = 125\text{ }^{\circ}C$			10	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 5V, V_{GS} = 10V$	3.5			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 4.5V, I_D = 3.5A$		43	50	m Ω
		$V_{GS} = 2.5V, I_D = 2A$		60	80	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 3.5A$		5		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 10V, f = 1MHz$		362		pF
Output Capacitance	C_{oss}			52		
Reverse Transfer Capacitance	C_{rss}			39		
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = 10V, V_{GS} = 4.5V,$ $I_D = 3.5A$		5.2		nC
Gate-Source Charge ^{1,2}	Q_{gs}			1.5		
Gate-Drain Charge ^{1,2}	Q_{gd}			1.8		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = 10V,$ $I_D = 1A, V_{GS} = 4.5V, R_{GS} = 6\Omega$		8		nS
Rise Time ^{1,2}	t_r			2.5		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			20		
Fall Time ^{1,2}	t_f			5		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_c = 25\text{ }^{\circ}C$)						
Continuous Current	I_S				2	A
Pulsed Current ³	I_{SM}				8	
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			1.2	V

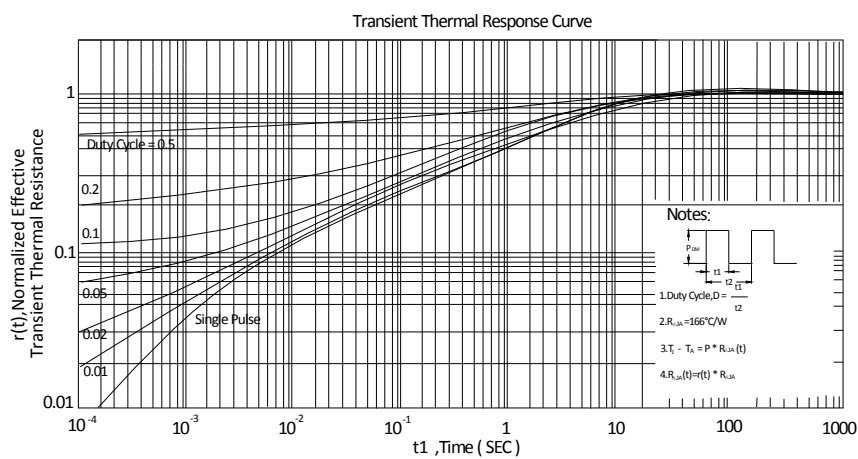
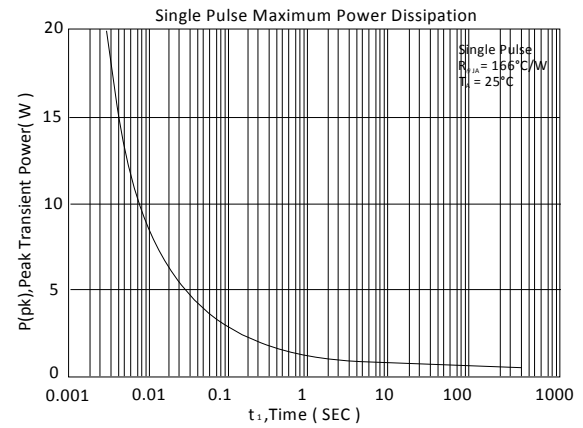
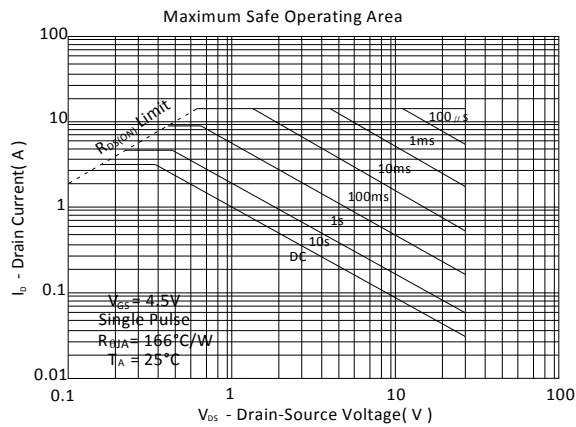
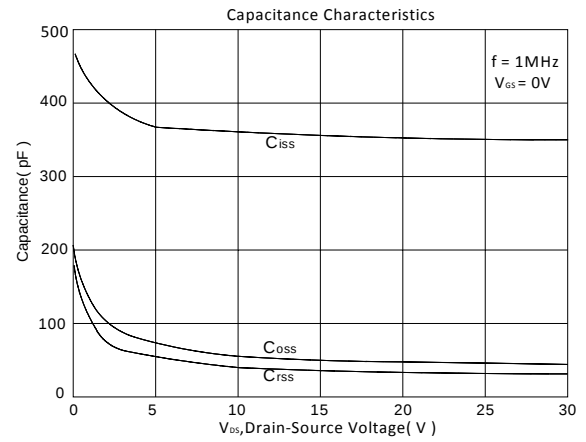
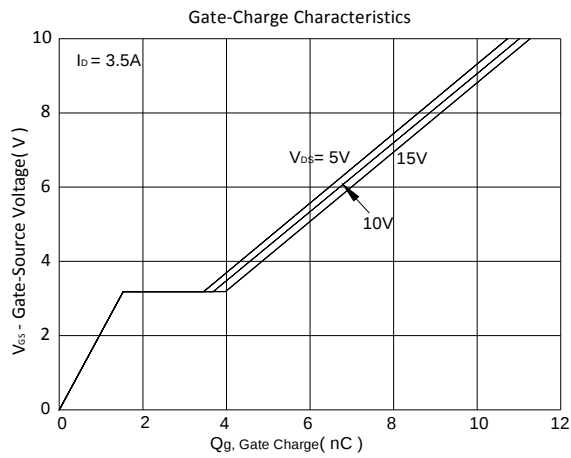
¹Pulse test : Pulse Width $\leq 300\text{ }\mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

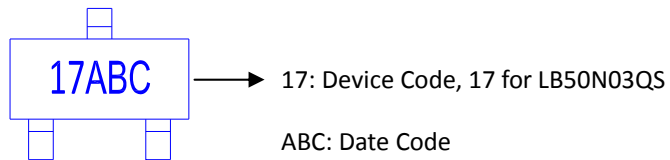
TYPICAL CHARACTERISTICS



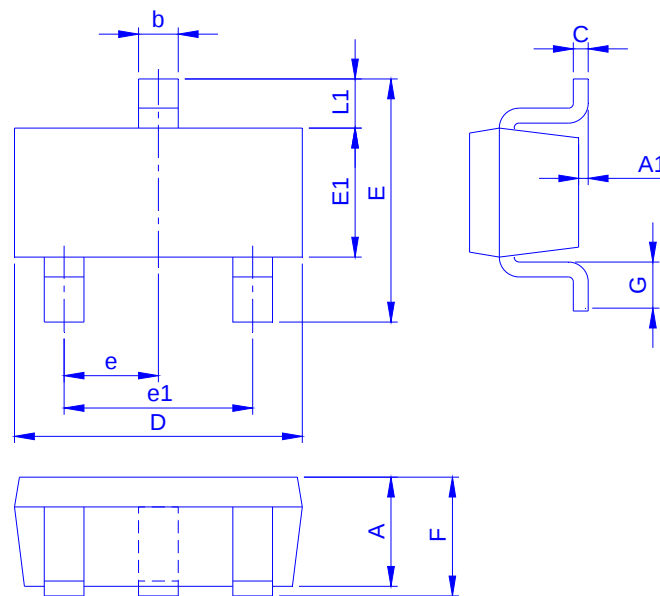


Ordering & Marking Information:

Device Name: LB50N03QS for SOT-23



Outline Drawing



Dimension in mm

Dimension	A	A1	b	C	D	E	E1	e	e1	F	G	L1
Min.	0.70	0	0.3	0.08	2.80	2.25	1.2	0.90		0.80	0.3	0.50
Typ.					2.90			0.95	1.9			
Max.	1.15	0.1	0.5	0.20	3.02	3.00	1.7	1.00		1.25	0.6	0.75

Footprint

