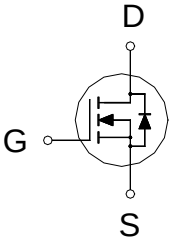
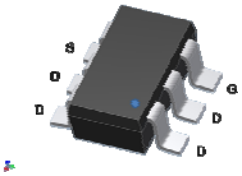
N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	30V
$R_{DSON\ (MAX.)}$	35mΩ
I_D	5.5A





Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A = 25 °C	I_D	5.5	A
	T_A = 70 °C		3.6	
Pulsed Drain Current[1]		I_{DM}	22	
Power Dissipation	T_A = 25 °C	P_D	1.25	W
	T_A = 70 °C		0.83	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Ambient	$R_{\theta JA}$		100	°C / W

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS (T_A = 25 °C, Unless Otherwise Noted)

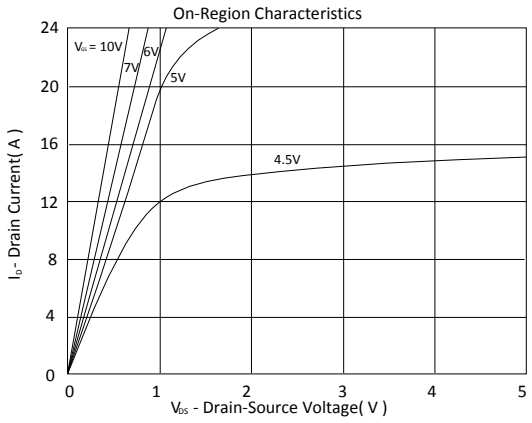
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.0	1.5	3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24V, V_{GS} = 0V			1	μA
		V_{DS} = 20V, V_{GS} = 0V, T_J = 125 °C			10	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5V, V_{GS} = 10V	5.5			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 5.5A		30	35	mΩ
		V_{GS} = 4.5V, I_D = 4.5A		40	50	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 5.5A		11		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 10V, f = 1MHz		323		pF
Output Capacitance	C_{oss}			75		
Reverse Transfer Capacitance	C_{rss}			53		
Total Gate Charge[1,2]	Q_g	V_{DS} = 10V, V_{GS} = 10V, I_D = 5.5A		7.1		nC
Gate-Source Charge[1,2]	Q_{gs}			1.1		
Gate-Drain Charge[1,2]	Q_{gd}			2.2		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = 15V, I_D = 1A, V_{GS} = 10V, R_{GS} = 6Ω		8		nS
Rise Time[1,2]	t_r			12		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			28		
Fall Time[1,2]	t_f			15		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				2	A
Pulsed Current[3]	I_{SM}				8	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			1.2	V

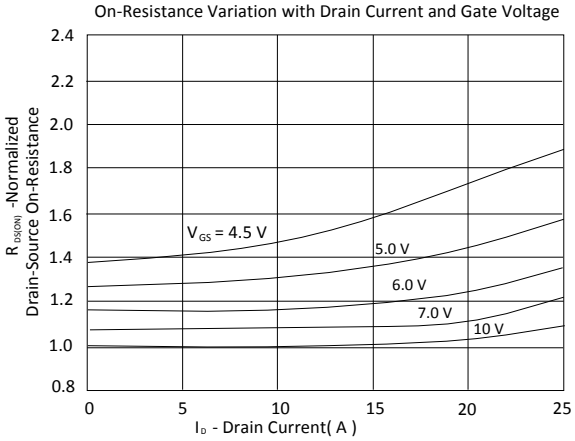
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

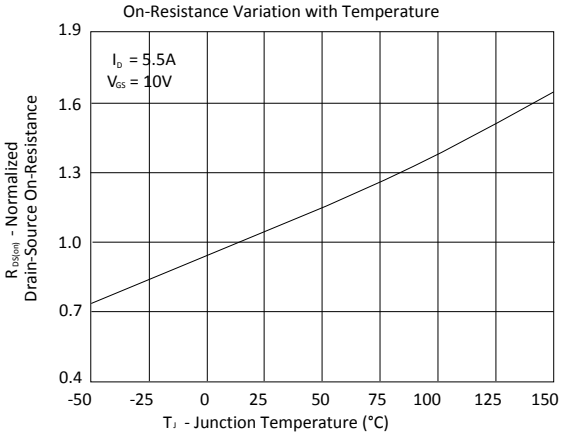
[2]Independent of operating temperature.

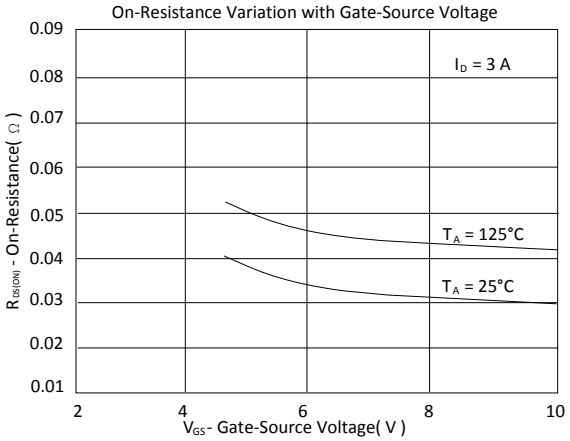
[3]Pulse width limited by maximum junction temperature.

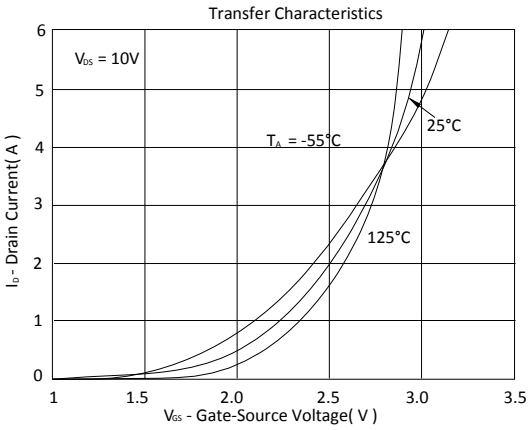
TYPICAL CHARACTERISTICS

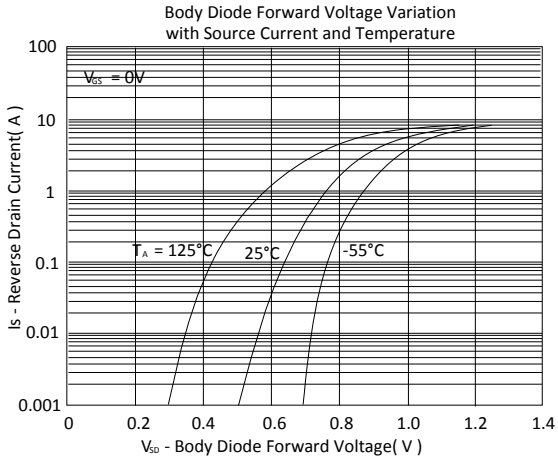




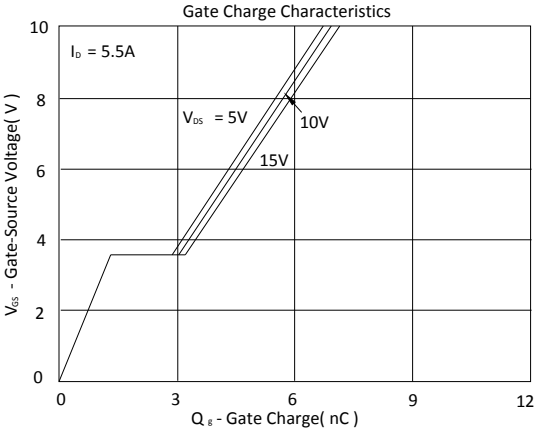




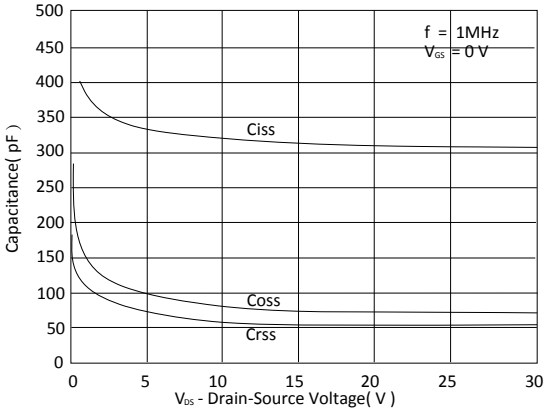




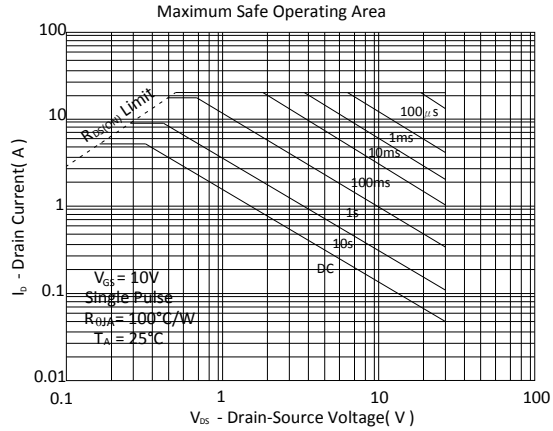
Gate Charge Characteristics



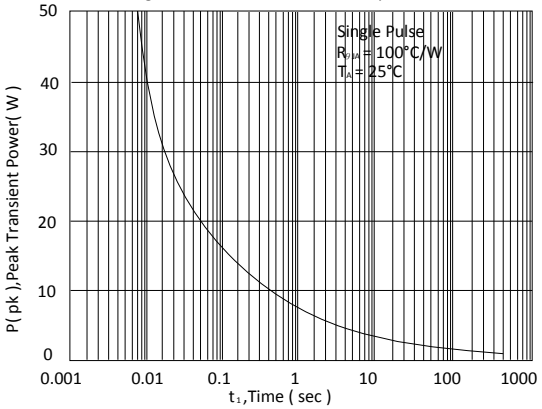
Capacitance Characteristics



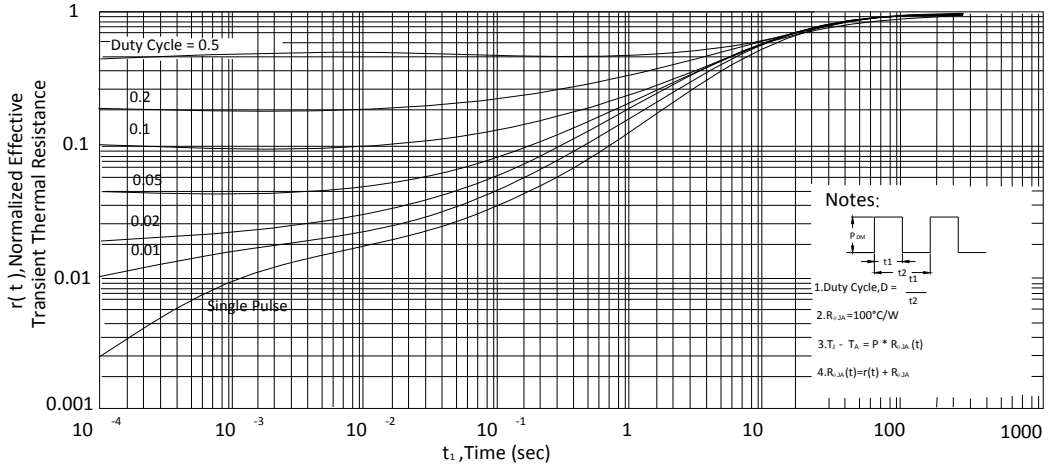
Maximum Safe Operating Area



Single Pulse Maximum Power Dissipation

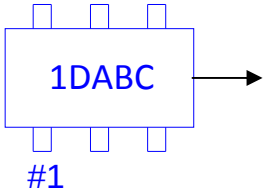


Transient Thermal Response Curve



Ordering & Marking Information:

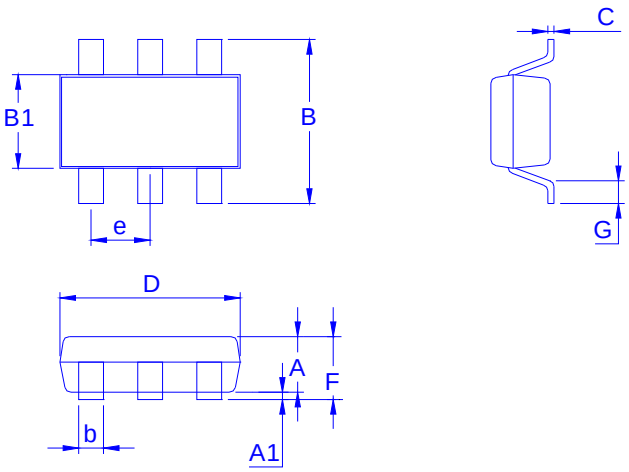
Device Name: LB32N03K for TSOP-6



1D: Device Code, 1D for LB32N03K

ABC: Date Code

Outline Drawing



Dimension in mm

Dimension	A	A1	B	B1	b	C	D	e	F	G
Min.	0.85	0	2.50	1.50	0.30	0.08	2.70		0.85	0.20
Typ.	0.95		2.80	1.60	0.40		2.90	0.95		
Max.	1.25	0.15	3.10	1.70	0.50	0.20	3.10		1.40	0.60

Footprint