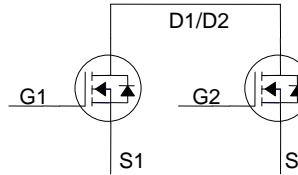


Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor
Product Summary:

BV_{DSS}	20V
$R_{DS(on)}$ (MAX.)	30mΩ
I_D	5A


Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current	$T_A = 25^\circ\text{C}$	I_D	5	A
	$T_A = 70^\circ\text{C}$		3.6	
Pulsed Drain Current ¹		I_{DM}	20	
Power Dissipation	$T_A = 25^\circ\text{C}$	P_D	1.25	W
	$T_A = 70^\circ\text{C}$		0.83	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Ambient	$R_{\theta JA}$		100	°C / W

¹Pulse width limited by maximum junction temperature.

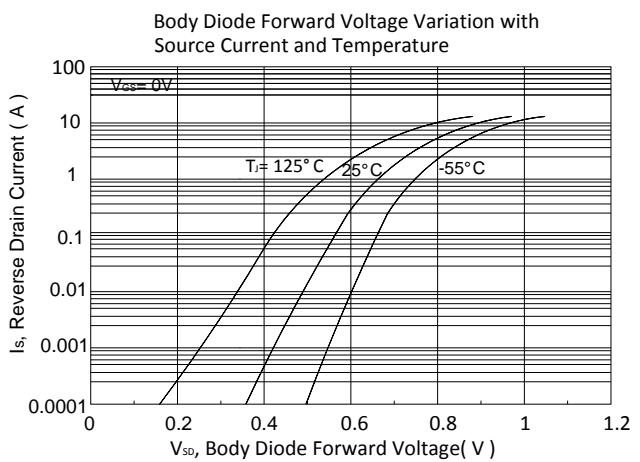
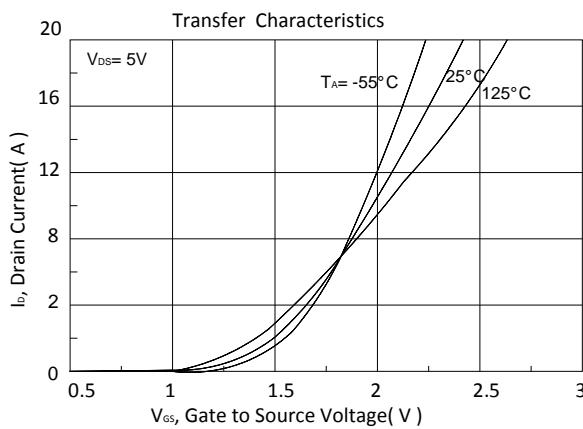
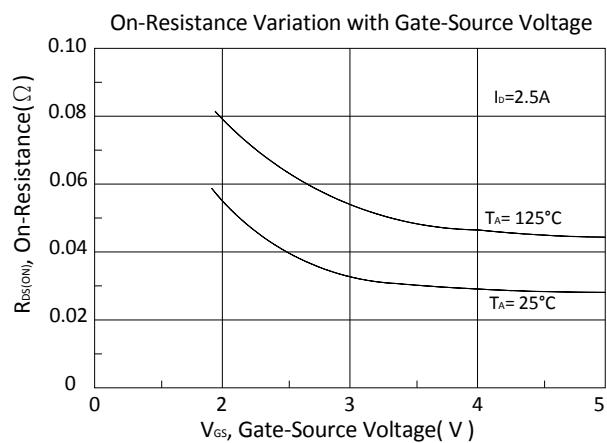
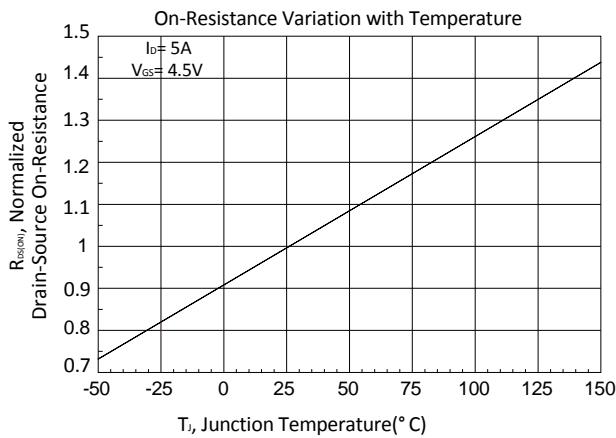
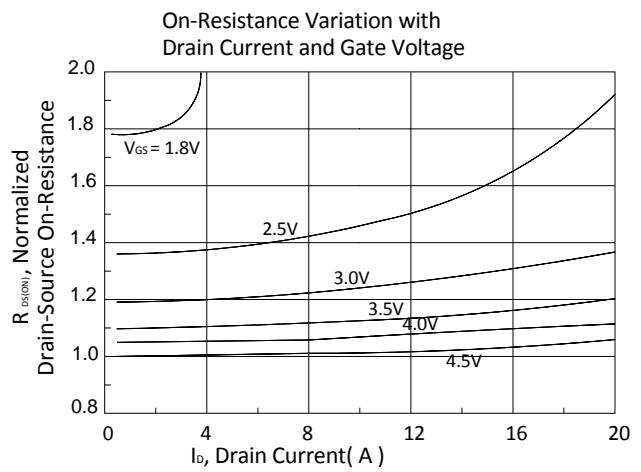
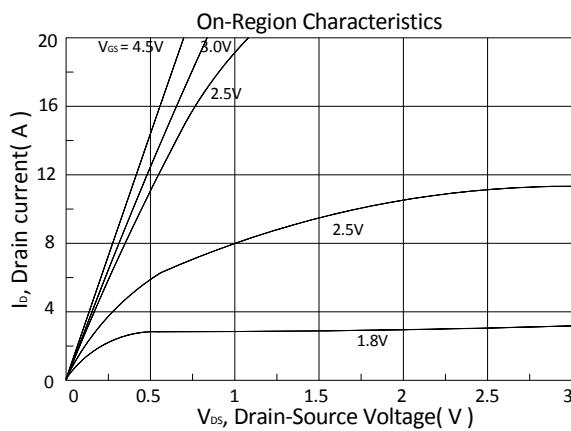
²Duty cycle ≤ 1%

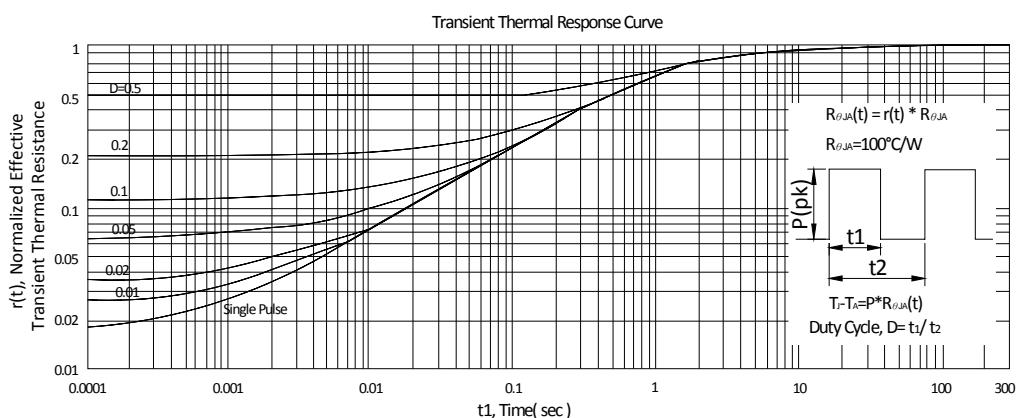
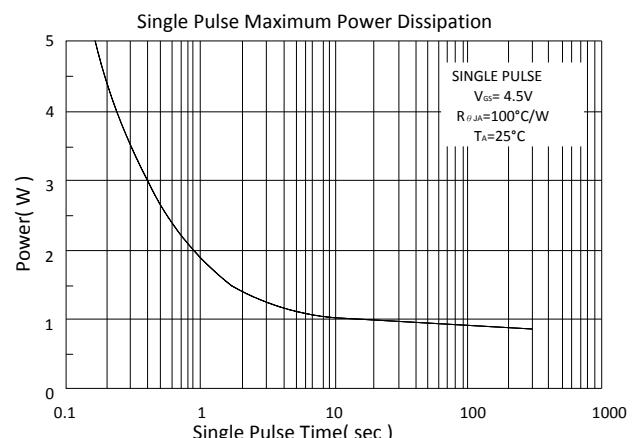
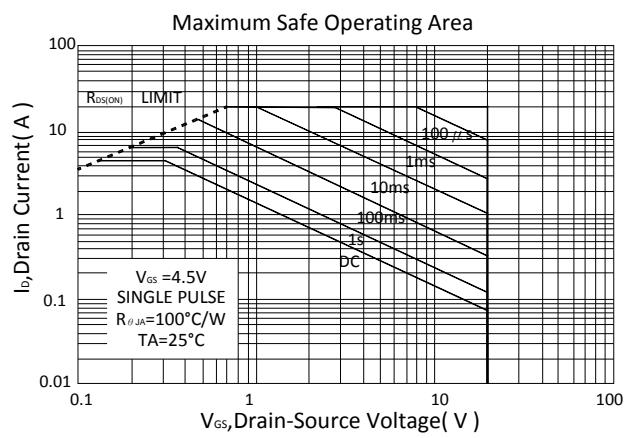
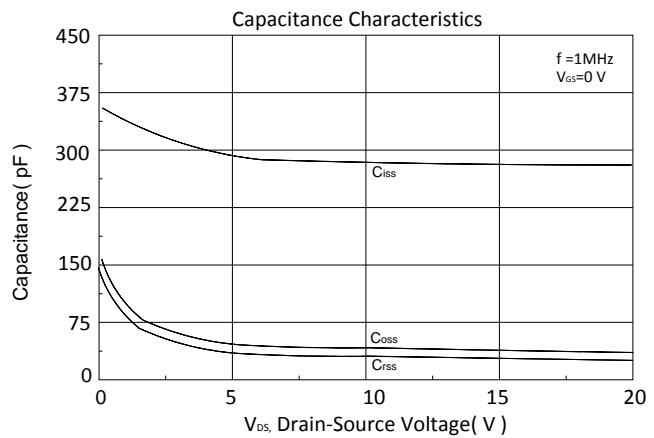
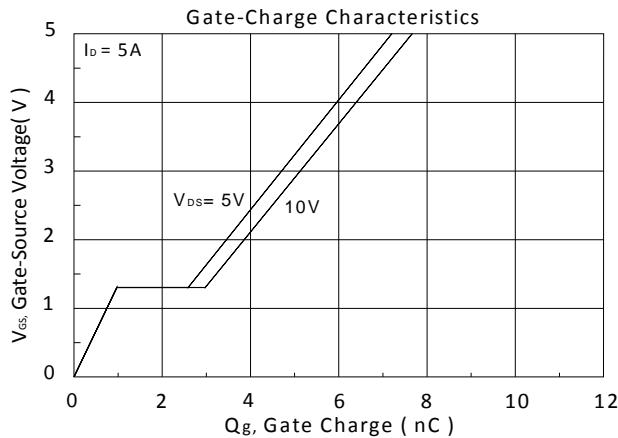
ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{GS} = 0V, I_D = 250\mu\text{A}$	20			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	0.45	0.75	1.2	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 12V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 16V, V_{GS} = 0V$			1	μA
		$V_{DS} = 16V, V_{GS} = 0V, T_J = 125^\circ\text{C}$			10	
On-State Drain Current ¹	$I_{D(\text{ON})}$	$V_{DS} = 5V, V_{GS} = 4.5V$	5			A
Drain-Source On-State Resistance ¹	$R_{DS(\text{ON})}$	$V_{GS} = 4.5V, I_D = 5A$		26	30	$\text{m}\Omega$
		$V_{GS} = 2.5V, I_D = 4A$		45	51	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 5A$		7		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 10V, f = 1\text{MHz}$		280		pF
Output Capacitance	C_{oss}			47		
Reverse Transfer Capacitance	C_{rss}			38		
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = 10V, V_{GS} = 4.5V, I_D = 5A$		6.2		nC
Gate-Source Charge ^{1,2}	Q_{gs}			0.9		
Gate-Drain Charge ^{1,2}	Q_{gd}			2.1		
Turn-On Delay Time ^{1,2}	$t_{d(\text{on})}$	$V_{DS} = 10V, I_D = 1A, V_{GS} = 4.5V, R_{GS} = 6\Omega$		12		nS
Rise Time ^{1,2}	t_r			15		
Turn-Off Delay Time ^{1,2}	$t_{d(\text{off})}$			30		
Fall Time ^{1,2}	t_f			13		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_c = 25^\circ\text{C}$)						
Continuous Current	I_S				2	A
Pulsed Current ³	I_{SM}				8	
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			1.2	V

¹Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.²Independent of operating temperature.³Pulse width limited by maximum junction temperature.

TYPICAL CHARACTERISTICS

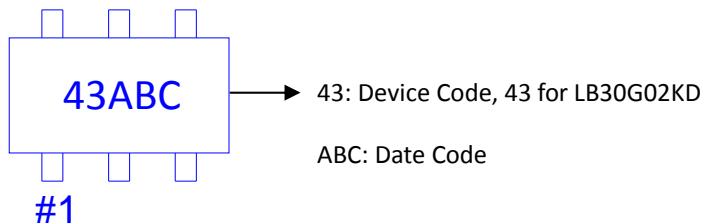




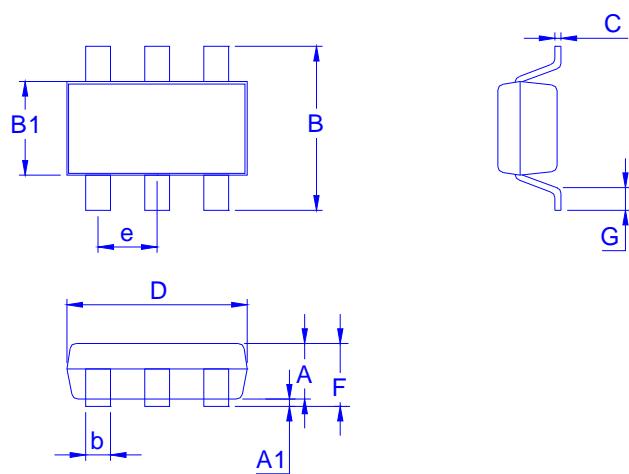
Ordering & Marking

Information:

Device Name: LB30G02KD for TSOP-6



Outline Drawing



Dimension in mm

Dimension	A	A1	B	B1	b	C	D	e	F	G
Min.	0.85	0	2.50	1.50	0.30	0.08	2.70		0.85	0.20
Typ.	0.95		2.80	1.60	0.40		2.90	0.95		
Max.	1.25	0.15	3.10	1.70	0.50	0.20	3.10		1.40	0.60

Footprint

