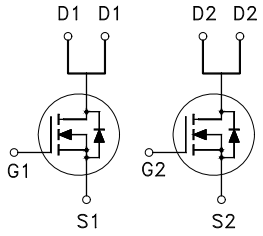
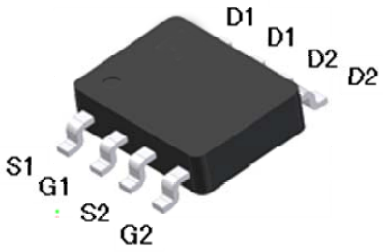
Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	20V
$R_{DSON\ (MAX.)}$	20mΩ
I_D	6A





UIS 100% Tested

Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current	T_A = 25 °C	I_D	6	A
	T_A = 100 °C		4	
Pulsed Drain Current[1]		I_{DM}	24	
Avalanche Current		I_{AS}	10	
Avalanche Energy	L = 0.1mH, ID=10A, RG=25Ω	E_{AS}	5	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	E_{AR}	2.5	
Power Dissipation	T_A = 25 °C	P_D	2	W
	T_A = 100 °C		0.8	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

100% UIS testing in condition of V_D=10V, L=0.1mH, V_G=4.5V, I_L=6A, Rated V_{DS}=20V N-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		25	°C / W
Junction-to-Ambient[3]	$R_{\theta JA}$		62.5	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

[3]62.5°C / W when mounted on a 1 in^2 pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	0.45	0.8	1.2	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16V, V_{GS} = 0V			1	μA
		V_{DS} = 16V, V_{GS} = 0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5V, V_{GS} = 4.5V	6			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 4.5V, I_D = 6A		17	20	mΩ
		V_{GS} = 2.5V, I_D = 5A		23	28	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 6A		8		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 10V, f = 1MHz		560		pF
Output Capacitance	C_{oss}			166		
Reverse Transfer Capacitance	C_{rss}			150		
Total Gate Charge[1,2]	Q_g	V_{DS} = 10V, V_{GS} = 4.5V, I_D = 6A		8.5		nC
Gate-Source Charge[1,2]	Q_{gs}			1.5		
Gate-Drain Charge[1,2]	Q_{gd}			3.5		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = 10V, I_D = 1A, V_{GS} = 4.5V, R_{GS} = 6Ω		12		nS
Rise Time[1,2]	t_r			15		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			30		
Fall Time[1,2]	t_f			13		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				2.3	A
Pulsed Current[3]	I_{SM}				9.2	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			1.2	V

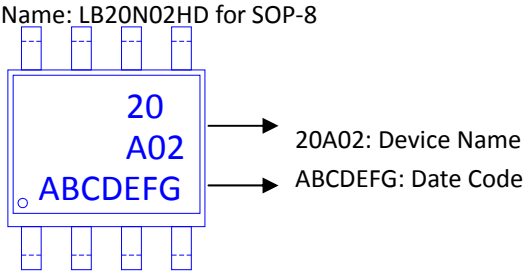
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

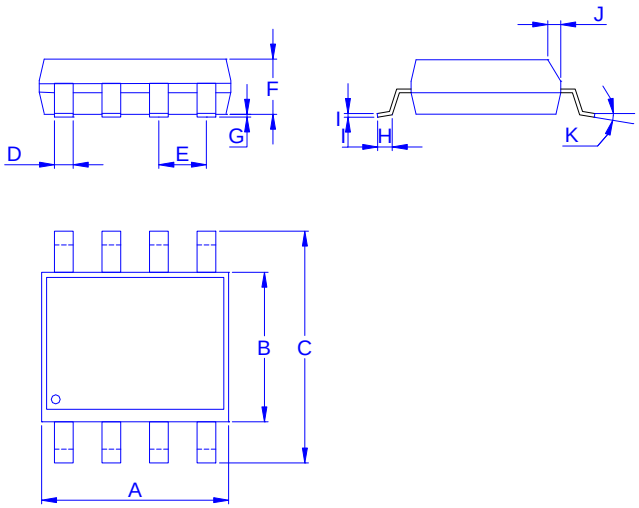
[3]Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: LB20N02HD for SOP-8

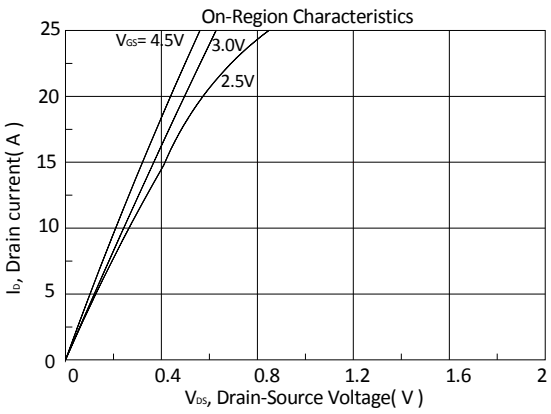


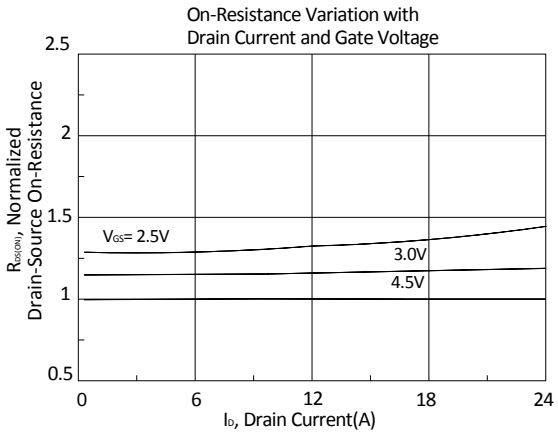
Outline Drawing

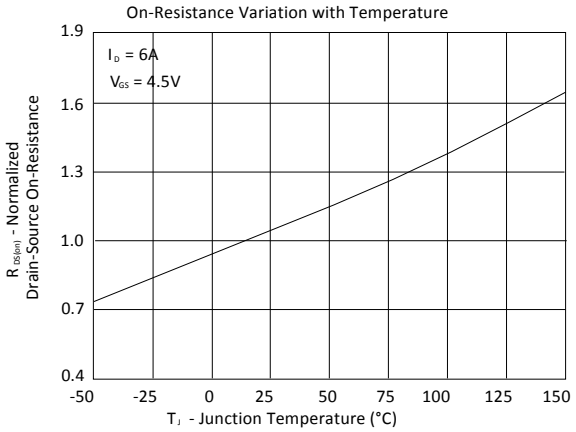


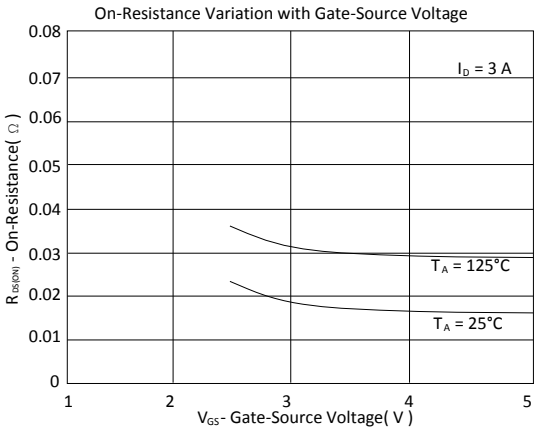
Dimension in mm

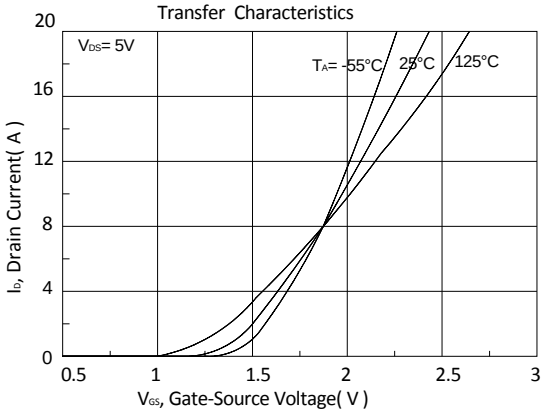
Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°

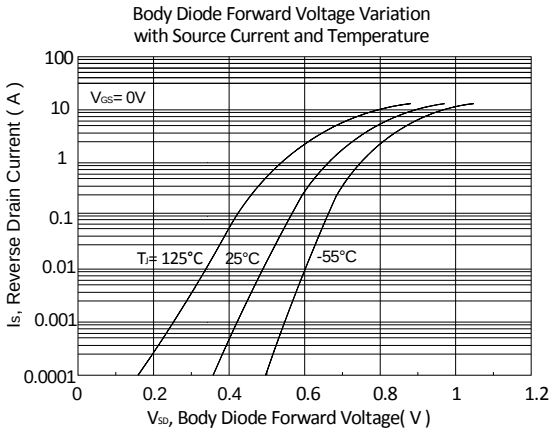

On-Region Characteristics
VGS= 4.5V
3.0V
2.5V
ID, Drain current(A)
VDS, Drain-Source Voltage(V)
0
5
10
15
20
25
0
0.4
0.8
1.2
1.6
2

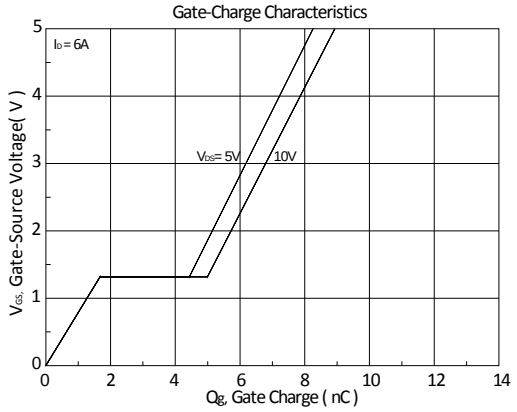

On-Resistance Variation with
Drain Current and Gate Voltage
RDS(ON), Normalized
Drain-Source On-Resistance
VGS= 2.5V
3.0V
4.5V
ID, Drain Current(A)
0.5
1
1.5
2
2.5
0
6
12
18
24

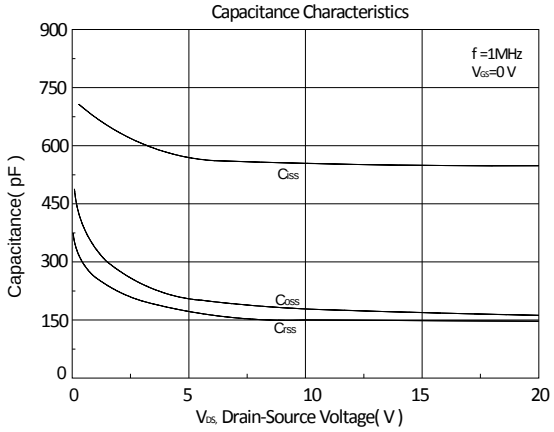

On-Resistance Variation with Temperature
ID = 6A
VGS = 4.5V
RDS(on) - Normalized
Drain-Source On-Resistance
TJ - Junction Temperature (°C)
0.4
0.7
1.0
1.3
1.6
1.9
-50
-25
0
25
50
75
100
125
150

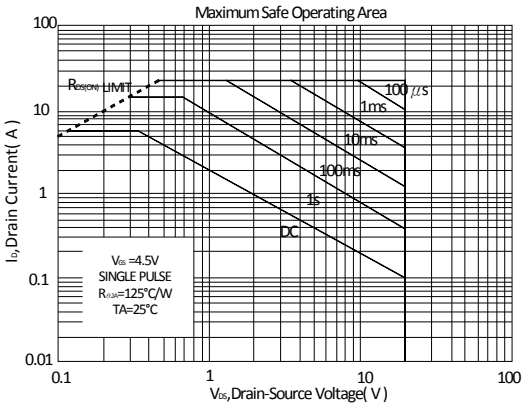

On-Resistance Variation with Gate-Source Voltage
ID = 3 A
TA = 125°C
TA = 25°C
RDS(ON) - On-Resistance(Ω)
VGS- Gate-Source Voltage(V)
0
0.01
0.02
0.03
0.04
0.05
0.06
0.07
0.08
1
2
3
4
5

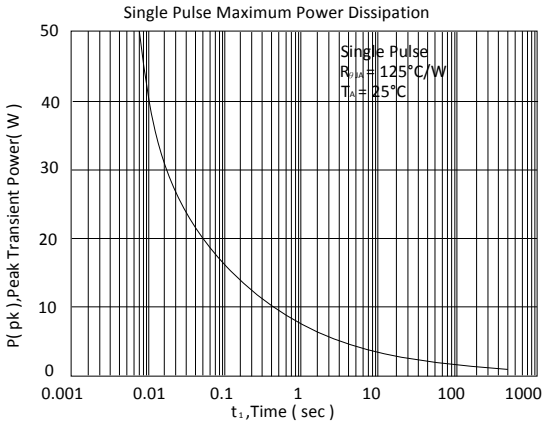

Transfer Characteristics
VDS= 5V
TA= -55°C
25°C
125°C
ID, Drain Current(A)
VGS, Gate-Source Voltage(V)
0
4
8
12
16
20
0.5
1
1.5
2
2.5
3

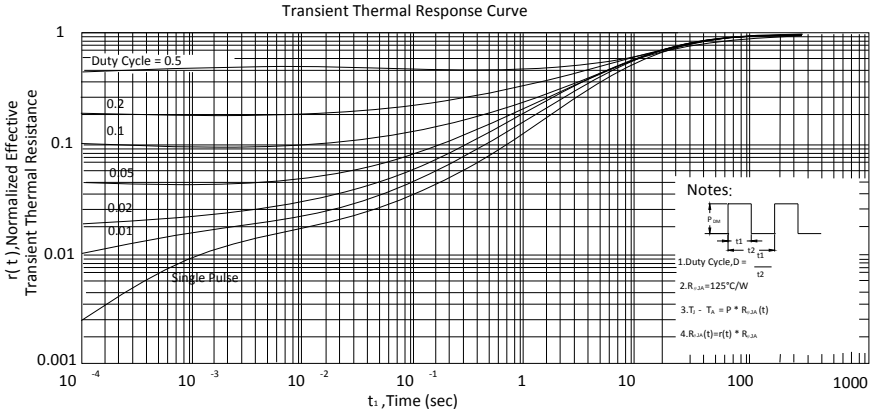

Body Diode Forward Voltage Variation
with Source Current and Temperature
VGS= 0V
TJ= 125°C
25°C
-55°C
IS, Reverse Drain Current (A)
VSD, Body Diode Forward Voltage(V)
0.0001
0.001
0.01
0.1
1
10
100
0
0.2
0.4
0.6
0.8
1
1.2


Gate-Charge Characteristics
I_D = 6A
V_DS= 5V
10V
V_GS, Gate-Source Voltage(V)
Qg, Gate Charge (nC)


Capacitance Characteristics
f =1MHz
V_GS=0 V
Ciss
Coss
Crss
Capacitance(pF)
V_DS, Drain-Source Voltage(V)


Maximum Safe Operating Area
R_DS(ON) LIMIT
100 μs
1ms
10ms
100ms
1s
DC
V_GS =4.5V
SINGLE PULSE
R_θJA=125°C/W
TA=25°C
I_D, Drain Current(A)
V_DS, Drain-Source Voltage(V)


Single Pulse Maximum Power Dissipation
Single Pulse
R_θJA = 125°C/W
TA = 25°C
P(pk),Peak Transient Power(W)
t1 ,Time (sec)


Transient Thermal Response Curve
Duty Cycle = 0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
Notes:
1.Duty Cycle,D = t1/t2
2.R_θJA=125°C/W
3.T_J - T_A = P * R_θJA (t)
4.R_θJA(t)=r(t) * R_θJA
r(t),Normalized Effective Transient Thermal Resistance
t1 ,Time (sec)