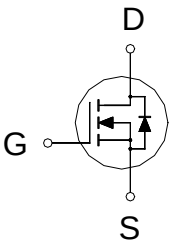
N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	60V
$R_{DSON\ (MAX.)}$	16mΩ
I_D	15A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A = 25 °C	I_D	15	A
	T_A = 100 °C		11	
Pulsed Drain Current[1]		I_{DM}	60	
Avalanche Current		I_{AS}	15	
Avalanche Energy	L = 0.1mH, ID=15A, RG=25Ω	E_{AS}	11.25	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	E_{AR}	5.62	
Power Dissipation	T_A = 25 °C	P_D	2.5	W
	T_A = 100 °C		1	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		6	°C / W
Junction-to-Ambient	$R_{\theta JA}$		50	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.0	2.0	3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48V, V_{GS} = 0V			1	μA
		V_{DS} = 40V, V_{GS} = 0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5V, V_{GS} = 10V	15			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 10A		13	16	mΩ
		V_{GS} = 4.5V, I_D = 5A		19	25	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 10A		25		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		2195		pF
Output Capacitance	C_{oss}			138		
Reverse Transfer Capacitance	C_{rss}			129		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz		1.4		Ω
Total Gate Charge[1,2]	Q_g	V_{DS} = 30V, V_{GS} = 10V, I_D = 10A		50		nC
Gate-Source Charge[1,2]	Q_{gs}			8.8		
Gate-Drain Charge[1,2]	Q_{gd}			14.7		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = 30V, I_D = 1A, V_{GS} = 10V, R_{GS} = 6Ω		20		nS
Rise Time[1,2]	t_r			15		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			50		
Fall Time[1,2]	t_f			20		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				15	A
Pulsed Current[3]	I_{SM}				60	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			1.3	V
Reverse Recovery Time	t_{rr}	I_F = 10A, dI_F/dt = 100A / μS		60		nS
Reverse Recovery Charge	Q_{rr}			42		nC

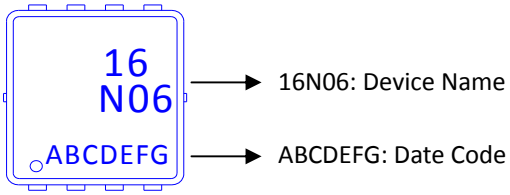
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

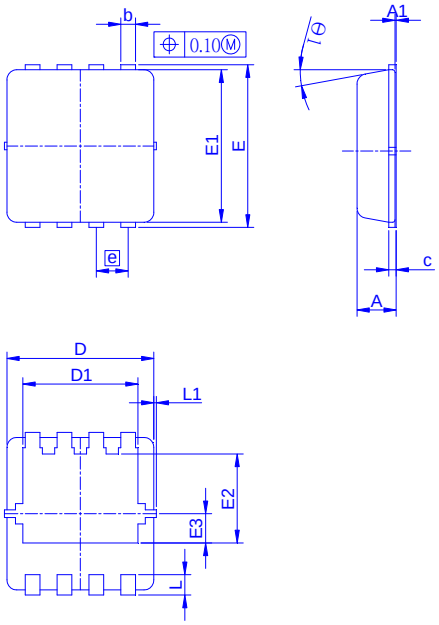
[3]Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: LB16N06B for EDFN 3 x 3



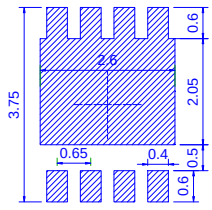
Outline Drawing



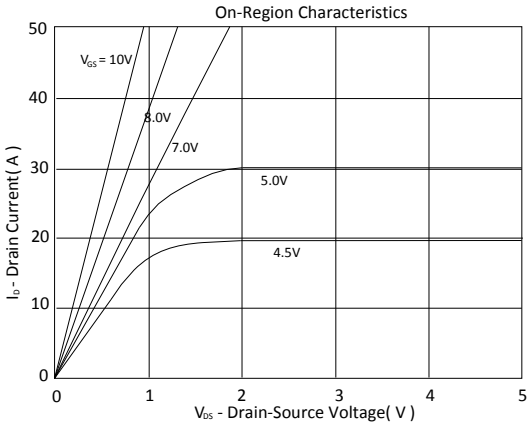
Dimension in mm

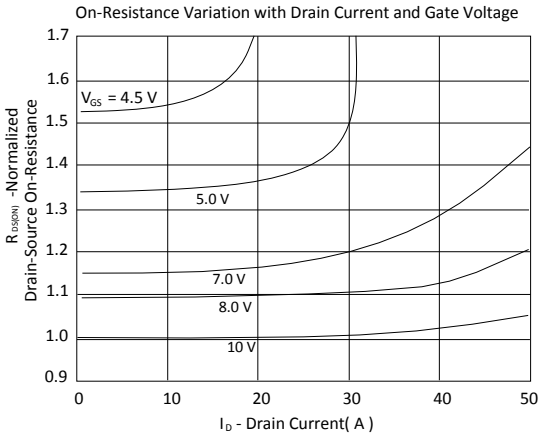
Dimension	A	A1	b	c	D	D1	E	E1	E2	E3	e	L	L1	Θ1
Min.	0.70	0	0.24	0.10	2.95	2.25	3.15	2.95	1.65			0.30		0°
Typ.	0.80		0.30	0.152	3.00	2.35	3.20	3.00	1.75	0.575	0.65	0.40	0.13	10°
Max.	0.90	0.05	0.37	0.25	3.15	2.45	3.40	3.15	1.96			0.50		12°

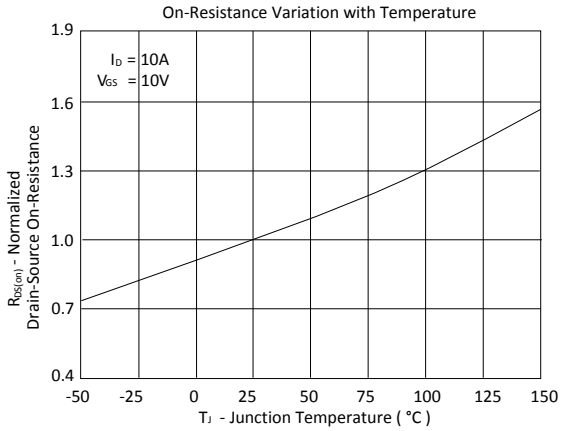
Recommended minimum pads

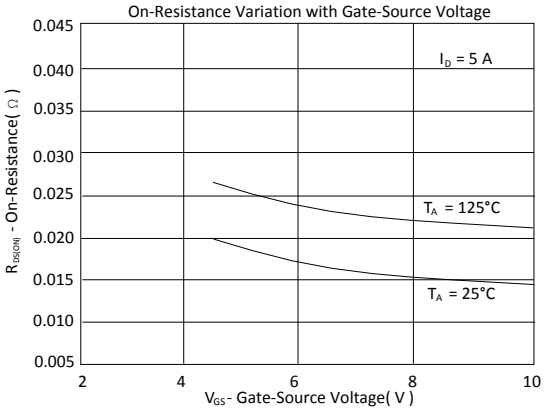


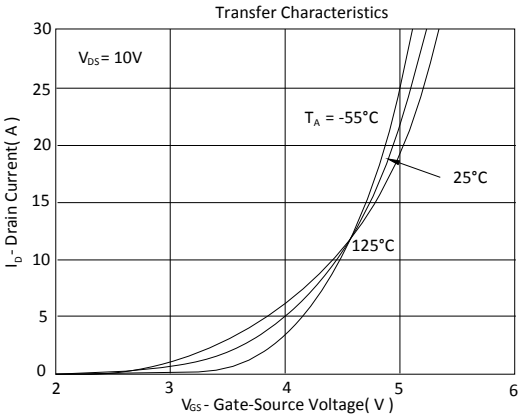
TYPICAL CHARACTERISTICS

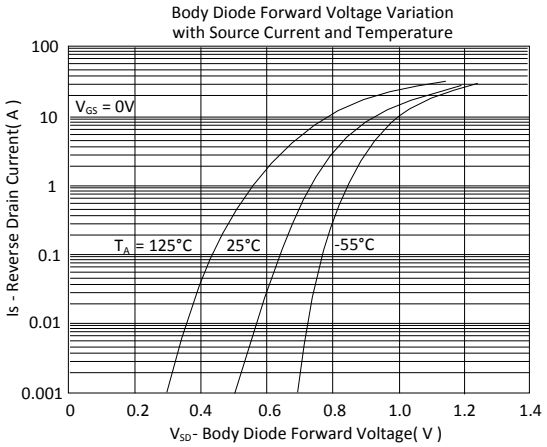




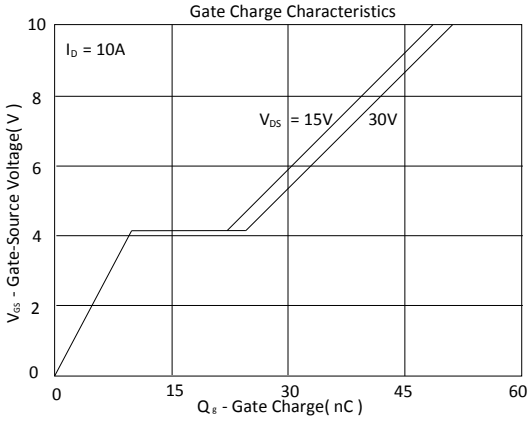




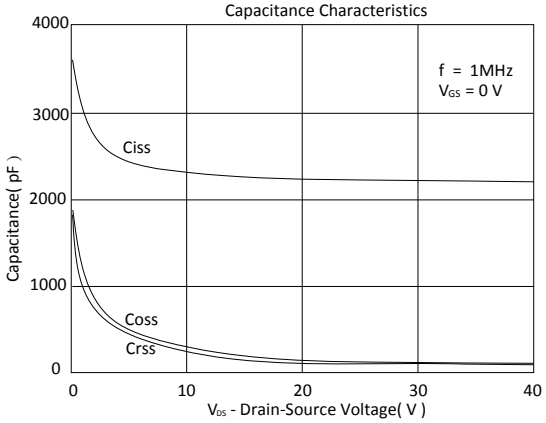




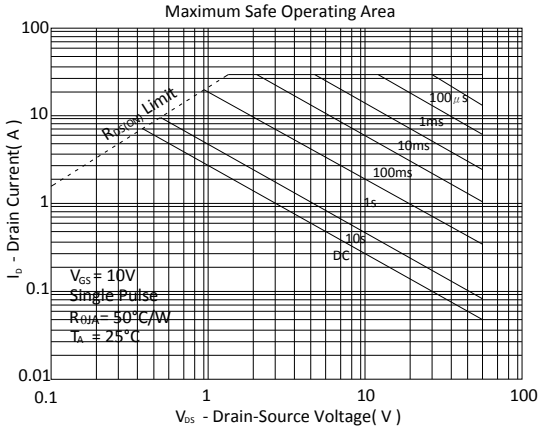
Gate Charge Characteristics



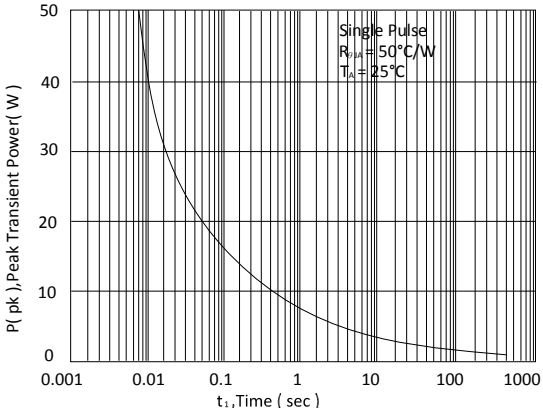
Capacitance Characteristics



Maximum Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve