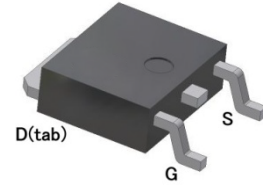
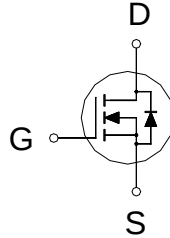


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	100V
$R_{DS(on)} (MAX.)$	12m Ω
I_D	68A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25\text{ }^{\circ}\text{C}$	I_D	68	A
	$T_C = 100\text{ }^{\circ}\text{C}$		43	
Pulsed Drain Current ¹		I_{DM}	150	
Avalanche Current		I_{AS}	18	mJ
Avalanche Energy	$L = 0.1\text{mH}, I_D = 18\text{A}, R_G = 25\Omega$	E_{AS}	16.2	
Repetitive Avalanche Energy ²	$L = 0.05\text{mH}$	E_{AR}	8.1	
Power Dissipation	$T_C = 25\text{ }^{\circ}\text{C}$	P_D	89	W
	$T_C = 100\text{ }^{\circ}\text{C}$		35	
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150	$^{\circ}\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		1.4	$^{\circ}\text{C} / \text{W}$
Junction-to-Ambient	$R_{\theta JA}$		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

ELECTRICAL CHARACTERISTICS (T_j = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	100			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.0	2.0	3.0	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80V, V _{GS} = 0V			1	μA
		V _{DS} = 70V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 5V, V _{GS} = 10V	68			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 10V, I _D = 12A		9.5	12	mΩ
		V _{GS} = 4.5V, I _D = 10A		11.5	15	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 12A		45		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 50V, f = 1MHz		2130		pF
Output Capacitance	C _{oss}			336		
Reverse Transfer Capacitance	C _{rss}			29		
Gate Resistance	R _g	V _{GS} = 15mV, V _{DS} = 0V, f = 1MHz		1.5		Ω
Total Gate Charge ^{1,2}	Q _g (V _{GS} =10V)	V _{DS} = 50V, V _{GS} = 10V, I _D = 12A		38		nC
	Q _g (V _{GS} =4.5V)			23		
Gate-Source Charge ^{1,2}	Q _{gs}			10		
Gate-Drain Charge ^{1,2}	Q _{gd}			8.2		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{DS} = 50V, I _D = 12A, V _{GS} = 10V, R _{GS} = 6Ω		6		nS
Rise Time ^{1,2}	t _r			10		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			8		
Fall Time ^{1,2}	t _f			25		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _c = 25 °C)						
Continuous Current	I _S				68	A
Pulsed Current ³	I _{SM}				150	
Forward Voltage ¹	V _{SD}	I _F = 12A, V _{GS} = 0V			1.2	V
Reverse Recovery Time	t _{rr}	I _F = 12A, dI _F /dt = 100A / μS		30		nS
Reverse Recovery Charge	Q _{rr}			130		nC

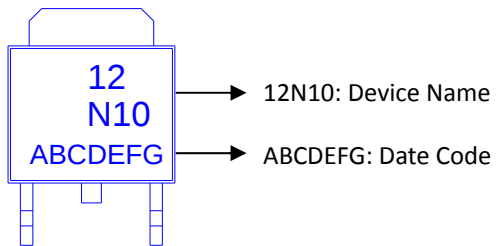
¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

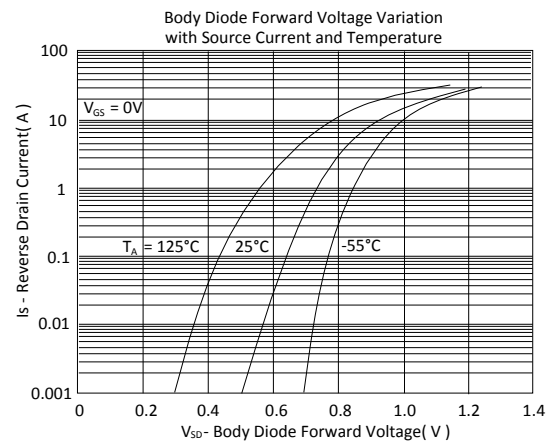
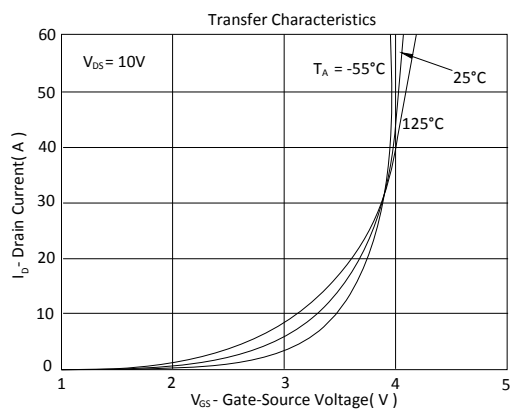
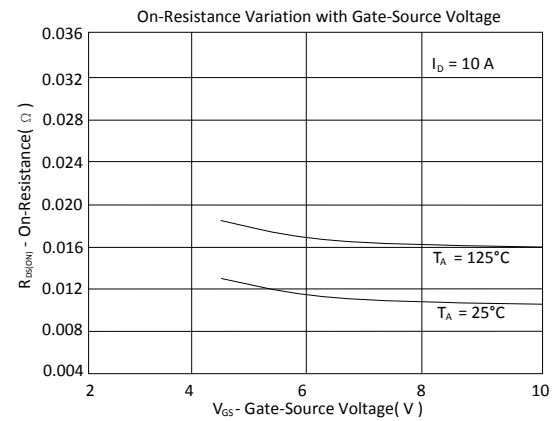
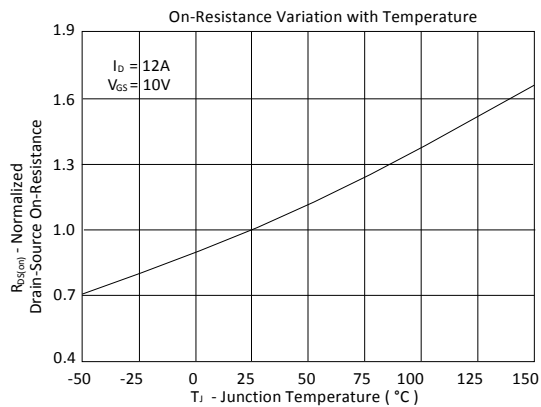
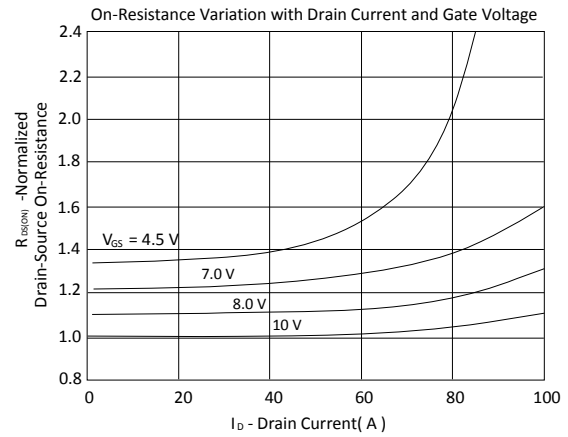
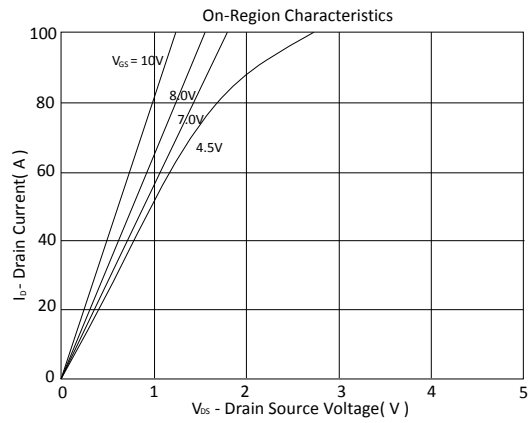
³Pulse width limited by maximum junction temperature.

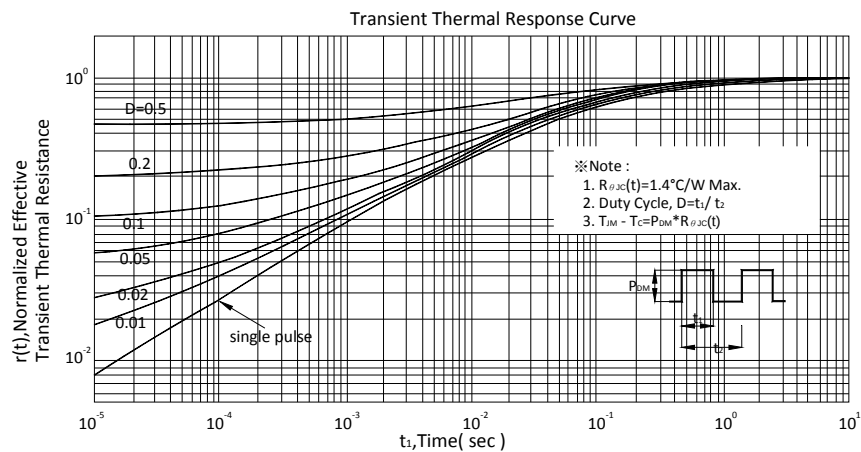
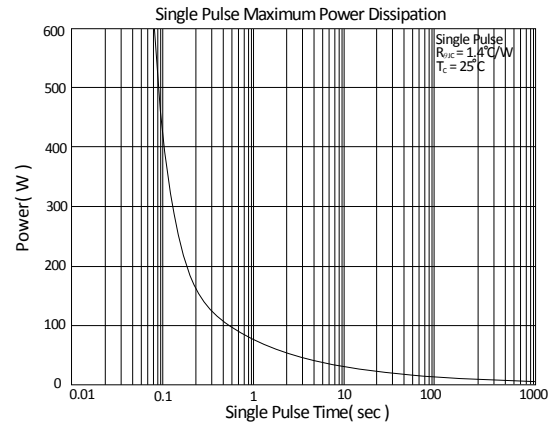
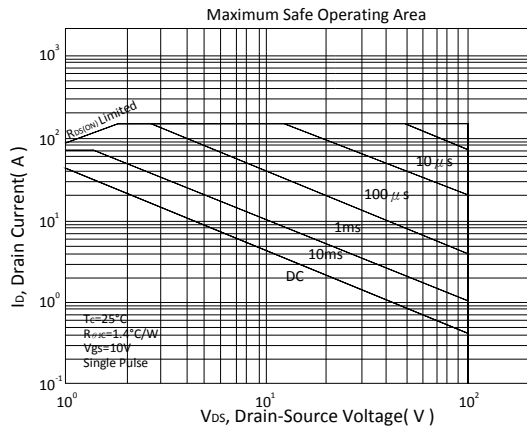
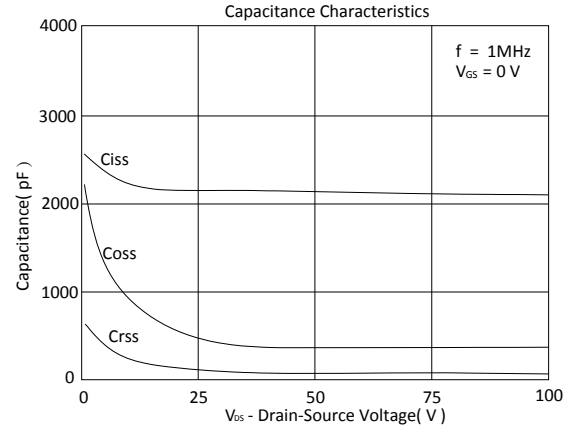
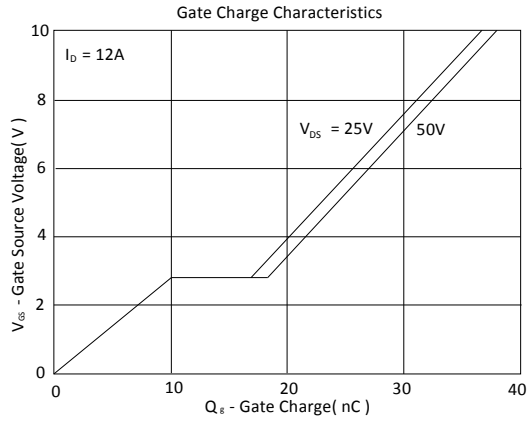
Ordering & Marking Information:

Device Name: LB12N10D for DPAK (TO-252)

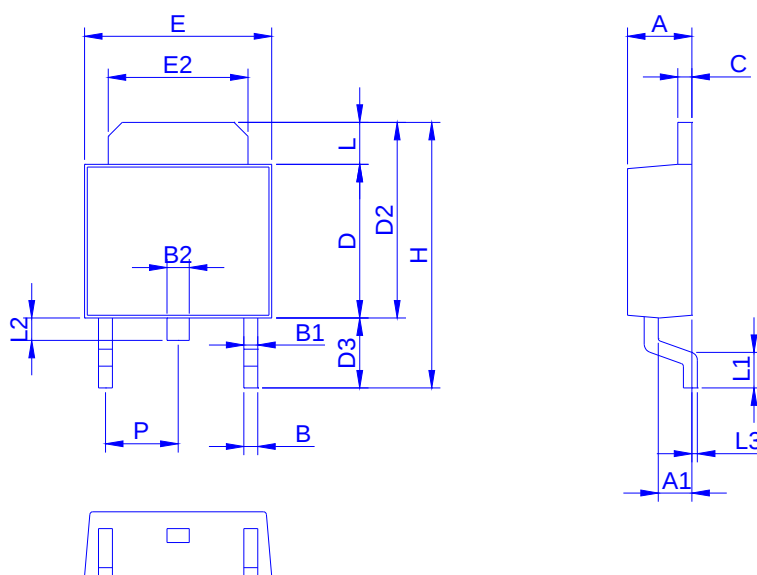


TYPICAL CHARACTERISTICS





Outline Drawing



Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	0.95	0.30	0.40	0.60	0.40	5.30	6.70	2.20	6.40	4.80	9.20	0.89	0.90	0.50	0.00	2.10
Max.	2.50	1.30	0.85	0.94	1.00	0.60	6.20	7.30	3.00	6.70	5.45	10.15	1.70	1.65	1.10	0.30	2.50

Footprint

