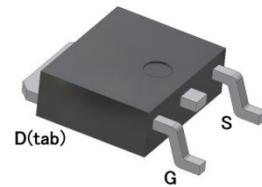
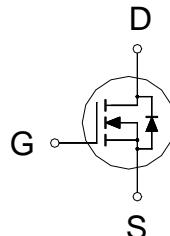


N-Channel Logic Level Enhancement Mode Field Effect Transistor
Product Summary:

BV_{DSS}	60V
$R_{DS(on)}$ (MAX.)	8mΩ
I_D	60A

UIS, R_g 100% Tested

Pb-Free Lead Plating & Halogen Free


ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	$T_C = 25^\circ C$	I_D	60	A
	$T_C = 100^\circ C$		35	
Pulsed Drain Current ^{1,3}		I_{DM}	170	
Avalanche Current		I_{AS}	60	
Avalanche Energy	$L = 0.1mH, I_D=60A, R_G=25\Omega$	E_{AS}	180	mJ
Repetitive Avalanche Energy ²	$L = 0.05mH$	E_{AR}	90	
Power Dissipation	$T_C = 25^\circ C$	P_D	50	W
	$T_C = 100^\circ C$		20	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

100% UIS testing in condition of $V_D=30V$, $L=0.1mH$, $V_G=10V$, $I_L=40A$, Rated $V_{DS}=60V$ N-CH
THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$	2.5	2.5	°C / W
Junction-to-Ambient	$R_{\theta JA}$		75	

¹Pulse width limited by maximum junction temperature.²Duty cycle ≤ 1%³Pulsed drain current rating is package limited.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)

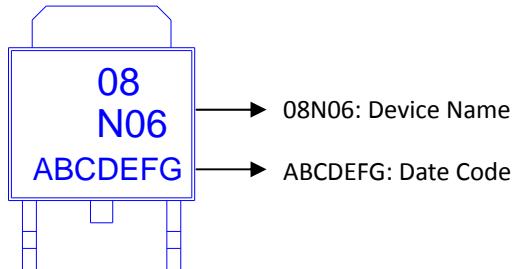
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{GS} = 0V, I_D = 250\mu\text{A}$	60			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1.0	2.0	3.0	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 48V, V_{GS} = 0V$			1	μA
		$V_{DS} = 40V, V_{GS} = 0V, T_J = 125^\circ\text{C}$			25	
On-State Drain Current ¹	$I_{D(\text{ON})}$	$V_{DS} = 5V, V_{GS} = 10V$	60			A
Drain-Source On-State Resistance ¹	$R_{DS(\text{ON})}$	$V_{GS} = 10V, I_D = 40A$		6.6	8.0	$\text{m}\Omega$
		$V_{GS} = 4.5V, I_D = 20A$		11	14	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 40A$		50		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 25V, f = 1\text{MHz}$		2869		pF
Output Capacitance	C_{oss}			296		
Reverse Transfer Capacitance	C_{rss}			68		
Gate Resistance	R_g	$V_{GS} = 15\text{mV}, V_{DS} = 0V, f = 1\text{MHz}$		2.0		Ω
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = 30V, V_{GS} = 10V, I_D = 40A$		38		nC
Gate-Source Charge ^{1,2}	Q_{gs}			17		
Gate-Drain Charge ^{1,2}	Q_{gd}			5.2		
Turn-On Delay Time ^{1,2}	$t_{d(\text{on})}$	$V_{DS} = 30V, I_D = 1A, V_{GS} = 10V, R_{GS} = 6\Omega$		20		nS
Rise Time ^{1,2}	t_r			80		
Turn-Off Delay Time ^{1,2}	$t_{d(\text{off})}$			120		
Fall Time ^{1,2}	t_f			100		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_c = 25^\circ\text{C}$)						
Continuous Current	I_S				60	A
Pulsed Current ³	I_{SM}				170	
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			1.3	V
Reverse Recovery Time	t_{rr}	$I_F = 25A, dI_F/dt = 100A / \mu\text{s}$		30		nS
Reverse Recovery Charge	Q_{rr}			150		

¹Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.²Independent of operating temperature.

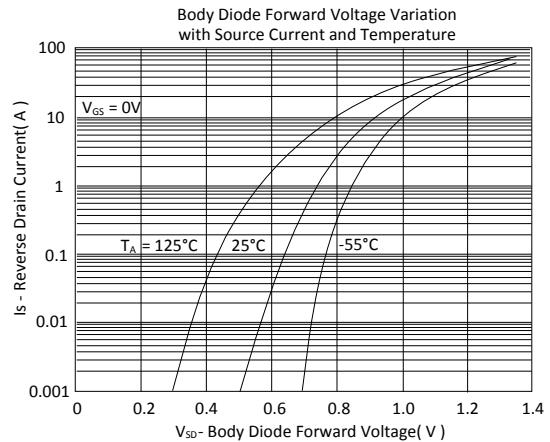
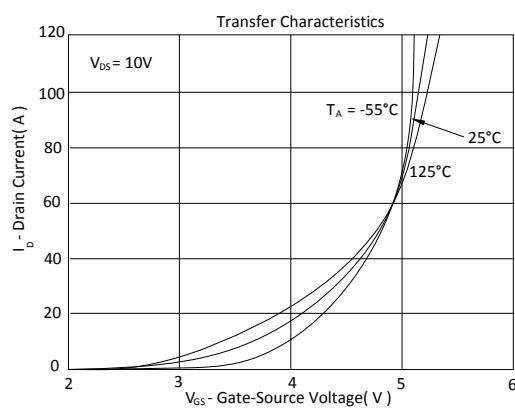
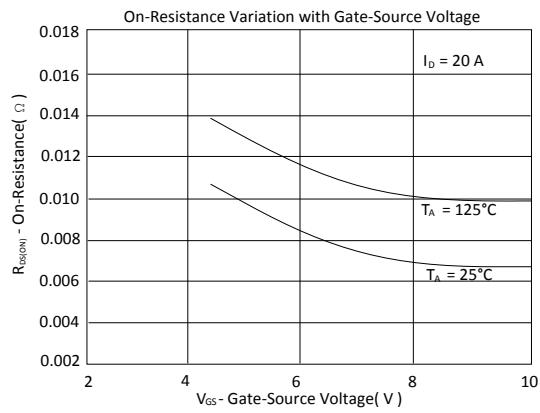
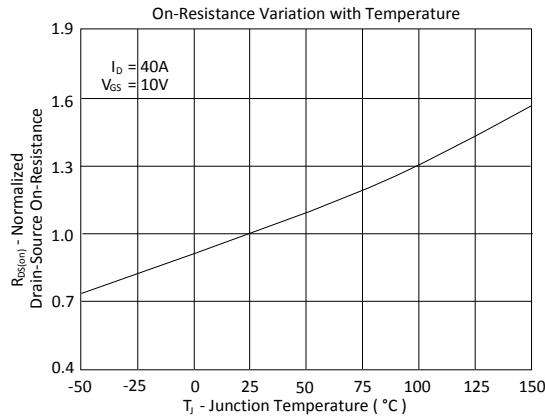
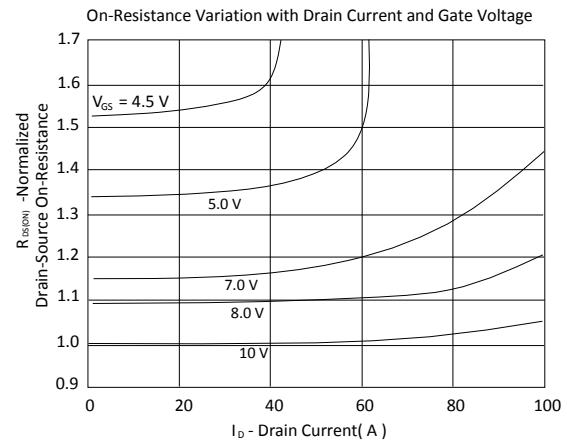
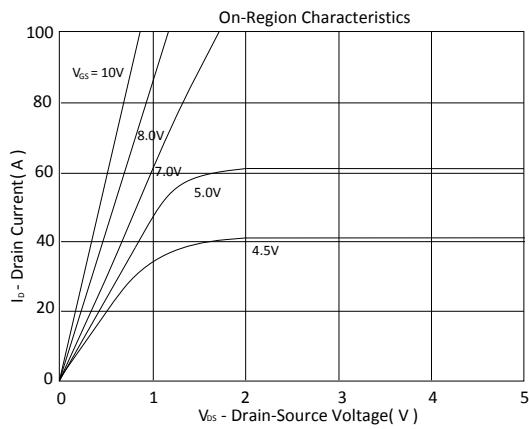
³Pulse width limited by maximum junction temperature.

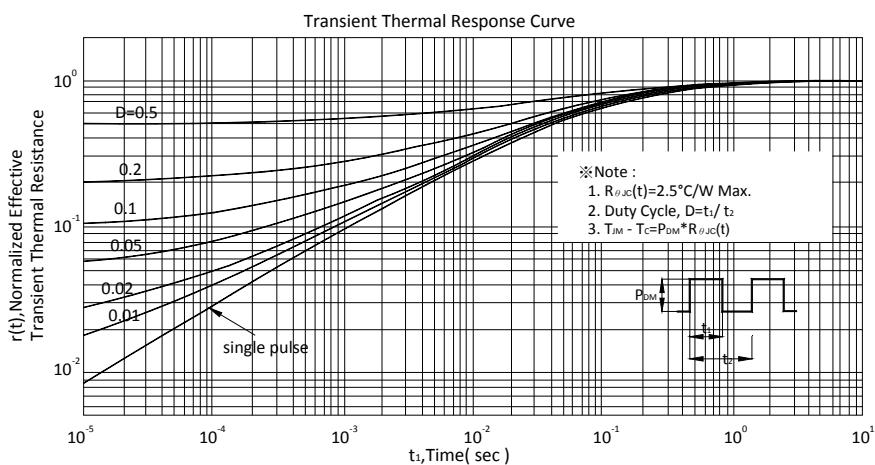
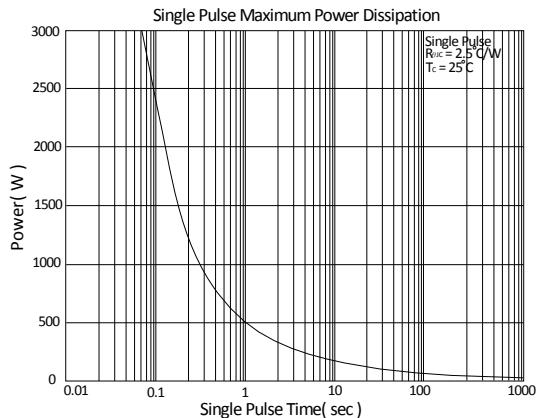
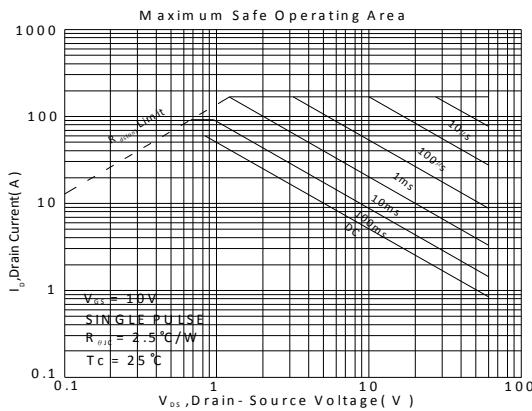
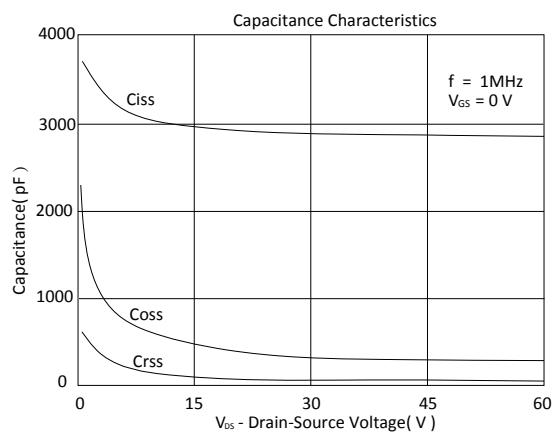
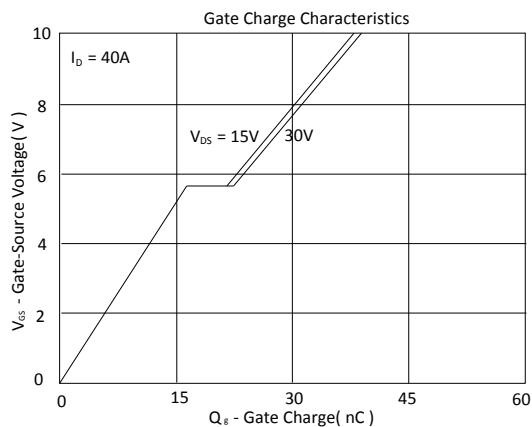
Ordering & Marking Information:

Device Name: LB08N06D for DPAK (TO-252)

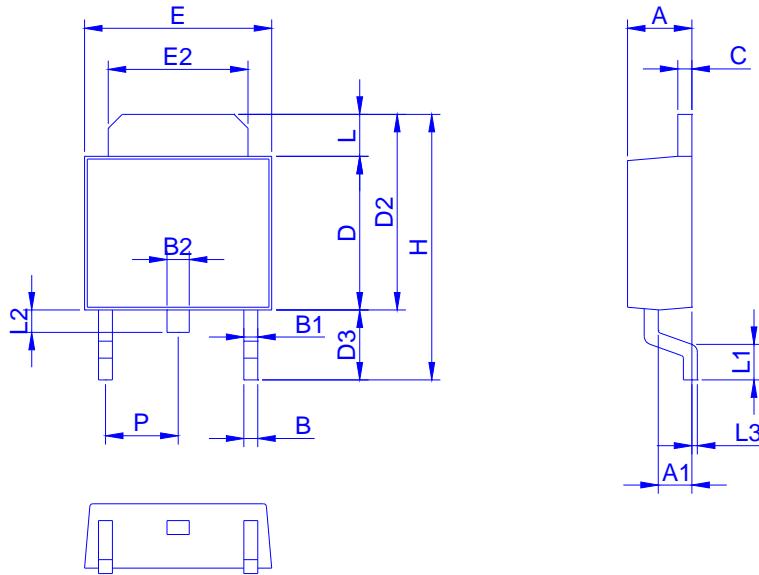


TYPICAL CHARACTERISTICS





Outline Drawing



Dimension in mm

Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	0.95	0.30	0.40	0.60	0.40	5.30	6.70	2.20	6.40	4.80	9.20	0.89	0.90	0.50	0.00	2.10
Max.	2.50	1.30	0.85	0.94	1.00	0.60	6.20	7.30	3.00	6.70	5.45	10.15	1.70	1.65	1.10	0.30	2.50

Footprint

