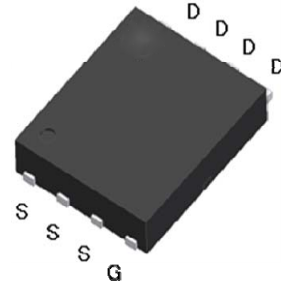


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	60V
R _{DS(on)} (MAX.)	8mΩ
I _D	60A



UIS, R_g 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _C = 25 °C	I _D	60	A
	T _C = 100 °C		35	
Pulsed Drain Current ^{1,3}		I _{DM}	170	
Avalanche Current		I _{AS}	60	mJ
Avalanche Energy	L = 0.1mH, I _D =60A, R _G =25Ω	E _{AS}	180	
Repetitive Avalanche Energy ²	L = 0.05mH	E _{AR}	90	
Power Dissipation	T _C = 25 °C	P _D	50	W
	T _C = 100 °C		20	
Operating Junction & Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C

100% UIS testing in condition of V_D=30V, L=0.1mH, V_G=10V, I_L=40A, Rated V_{DS}=60V N-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}		2.5	°C / W
Junction-to-Ambient	R _{θJA}		75	

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

³Pulsed drain current rating is package limited.

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.0	2.0	3.0	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 48V, V_{GS} = 0V$			1	μA
		$V_{DS} = 40V, V_{GS} = 0V, T_J = 125\text{ }^{\circ}C$			25	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 5V, V_{GS} = 10V$	60			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 40A$		6.6	8.0	m Ω
		$V_{GS} = 4.5V, I_D = 20A$		11	14	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 40A$		50		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 25V, f = 1MHz$		2869		pF
Output Capacitance	C_{oss}			296		
Reverse Transfer Capacitance	C_{rss}			68		
Gate Resistance	R_g	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		2.0		Ω
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = 30V, V_{GS} = 10V,$ $I_D = 40A$		38		nC
Gate-Source Charge ^{1,2}	Q_{gs}			17		
Gate-Drain Charge ^{1,2}	Q_{gd}			5.2		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = 30V,$ $I_D = 1A, V_{GS} = 10V, R_{GS} = 6\Omega$		20		nS
Rise Time ^{1,2}	t_r			80		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			120		
Fall Time ^{1,2}	t_f			100		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _C = 25 °C)						
Continuous Current	I_S				60	A
Pulsed Current ³	I_{SM}				170	
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			1.3	V
Reverse Recovery Time	t_{rr}	$I_F = 25A, dI_F/dt = 100A / \mu S$		30		nS
Reverse Recovery Charge	Q_{rr}			150		nC

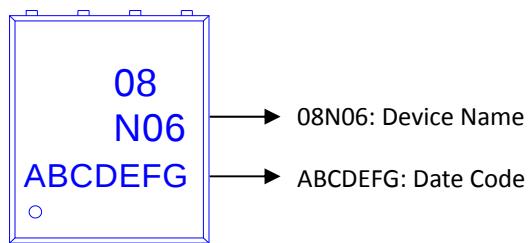
¹Pulse test : Pulse Width $\leq 300\text{ }\mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

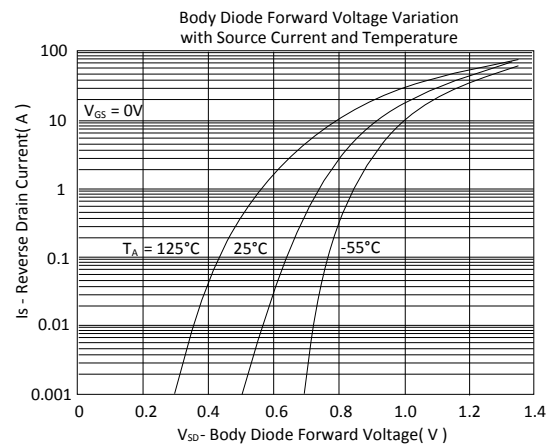
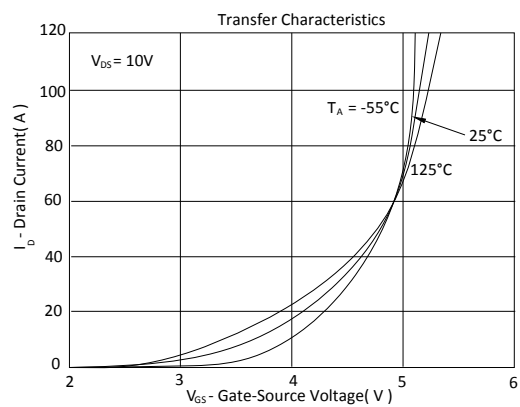
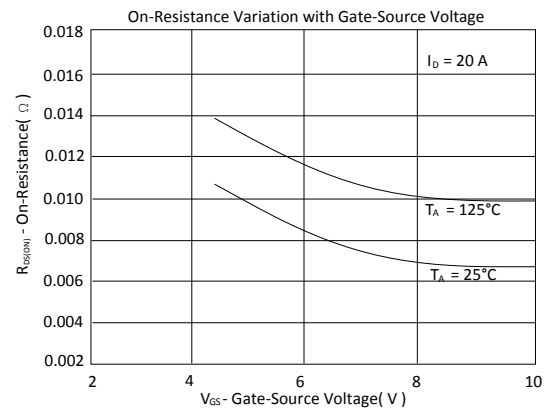
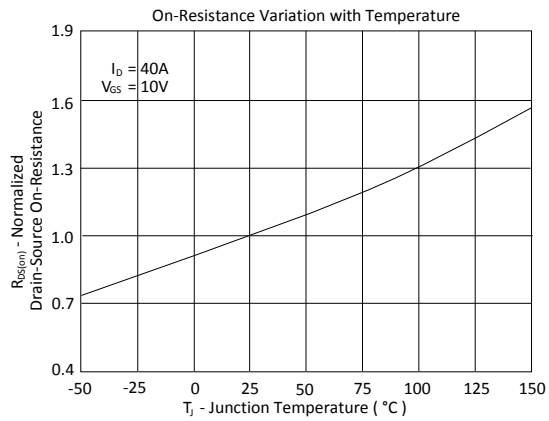
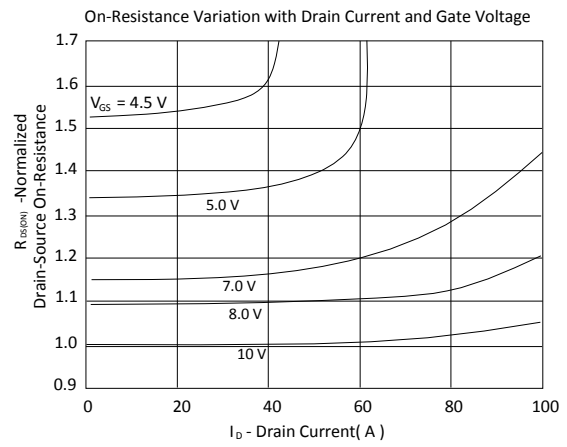
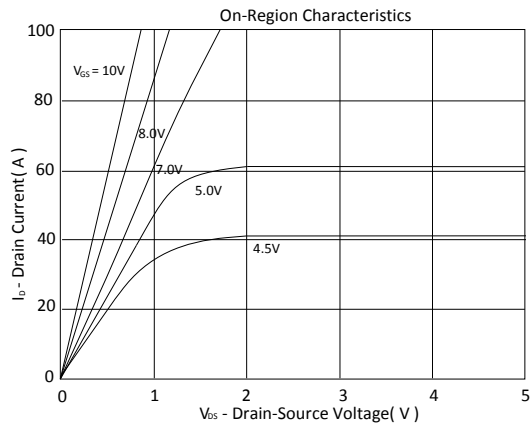
³Pulse width limited by maximum junction temperature.

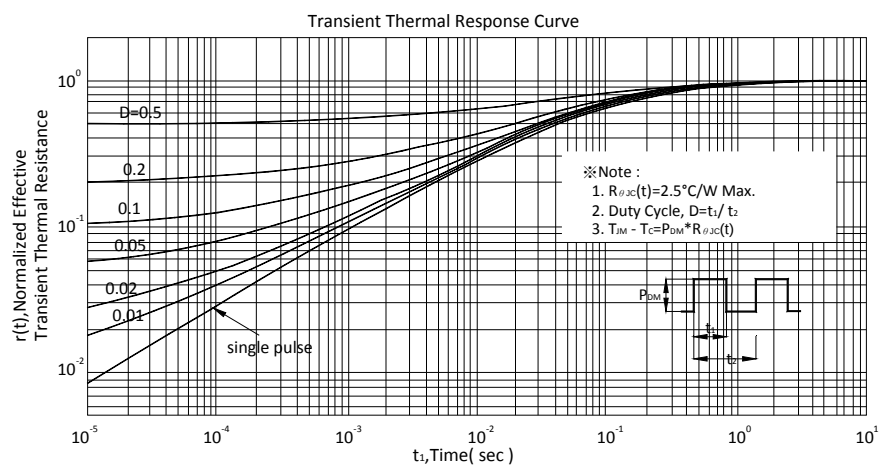
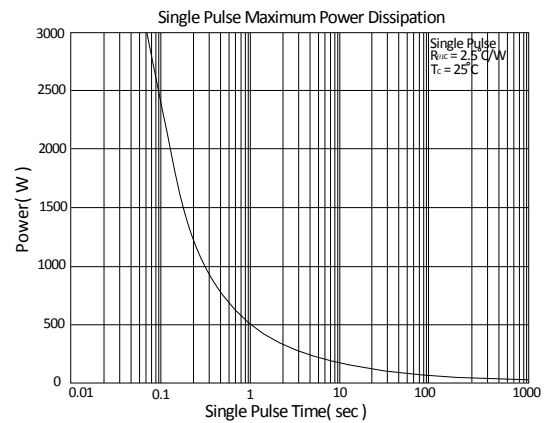
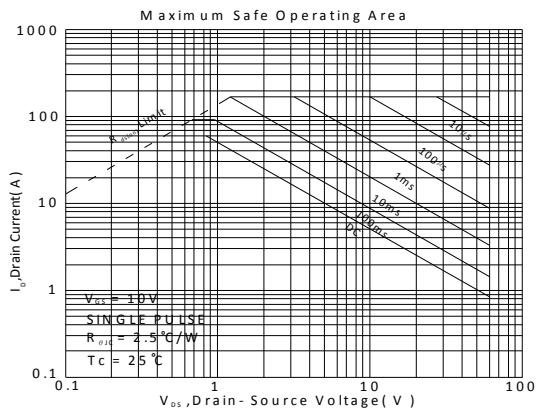
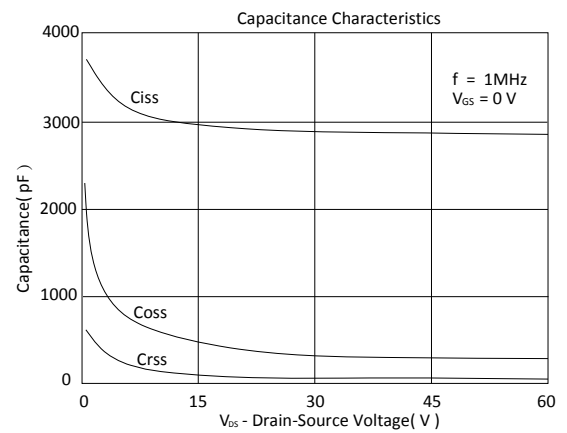
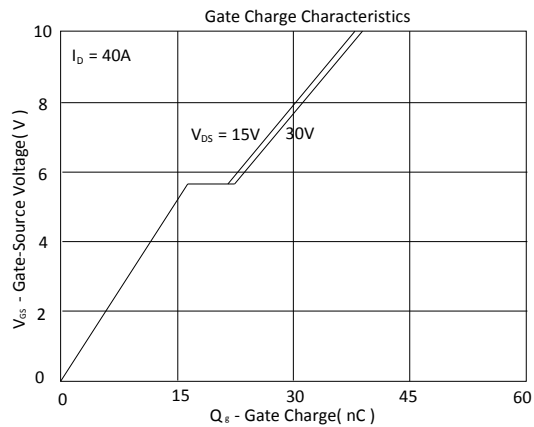
Ordering & Marking Information:

Device Name: LB08N06C for EDFN 5 x 6

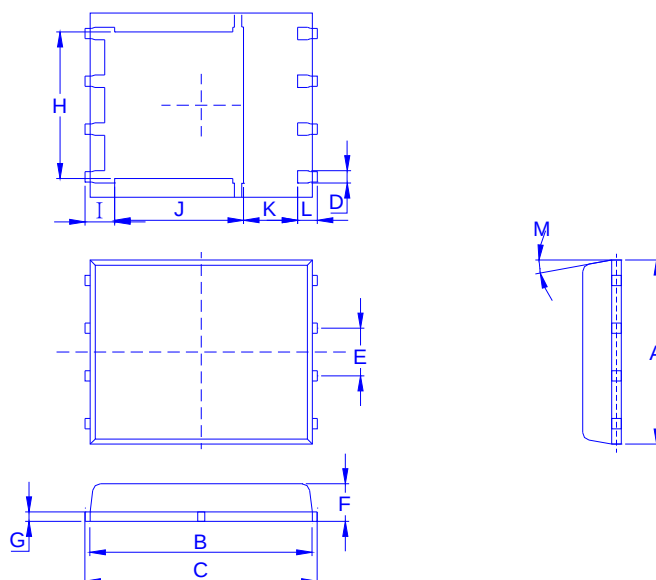


TYPICAL CHARACTERISTICS





Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K	L	M
Min.	4.80	5.50	5.90	0.3		0.85	0.15	3.67	0.41	3.00	0.94	0.45	0°
Typ.					1.27								
Max.	5.30	5.90	6.15	0.51		1.20	0.30	4.54	0.85	3.92	1.7	0.71	12°

Recommended minimum pads

