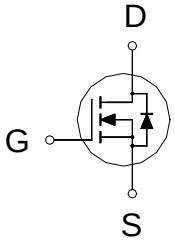
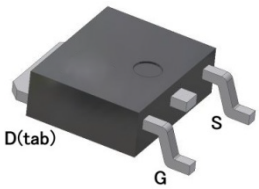
N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	15V
$R_{DSON\ (MAX.)}$	7mΩ
I_D	65A





UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current	T_C = 25 °C	I_D	65	A
	T_C = 100 °C		41	
Pulsed Drain Current[1]		I_{DM}	160	
Avalanche Current		I_{AS}	35	
Avalanche Energy	L = 0.1mH, I_D=35A, R_G=25Ω	E_{AS}	61.25	mJ
Power Dissipation	T_C = 25 °C	P_D	50	W
	T_C = 100 °C		20	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

100% UIS testing in condition of V_D=15V, L=0.1mH, V_G=10V, I_L=20A, Rated V_{DS}=15V N-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		2.5	°C / W
Junction-to-Ambient[3]	$R_{\theta JA}$		75	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

[3]75°C / W when mounted on a 1 in^2 pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	15			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	0.35	0.6	0.9	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±8V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 12V, V_{GS} = 0V			1	μA
		V_{DS} = 10V, V_{GS} = 0V, T_J = 125 °C			10	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5V, V_{GS} = 4.5V	65			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 4.5V, I_D = 18A		5.8	7	mΩ
		V_{GS} = 2.5V, I_D = 15A		6.5	8	
		V_{GS} = 1.8V, I_D = 10A		7.5	10	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 18A		22		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 10V, f = 1MHz		2091		pF
Output Capacitance	C_{oss}			250		
Reverse Transfer Capacitance	C_{rss}			172		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz		1.8		Ω
Total Gate Charge[1,2]	Q_g	V_{DS} = 10V, V_{GS} = 4.5V, I_D = 18A		19		nC
Gate-Source Charge[1,2]	Q_{gs}			2.3		
Gate-Drain Charge[1,2]	Q_{gd}			4		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = 10V, I_D = 1A, V_{GS} = 4.5V, R_{GS} = 6Ω		10		nS
Rise Time[1,2]	t_r			15		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			50		
Fall Time[1,2]	t_f			18		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				65	A
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			1.3	V
Reverse Recovery Time	t_{rr}			30		nS
Reverse Recovery Charge	Q_{rr}			20		nC

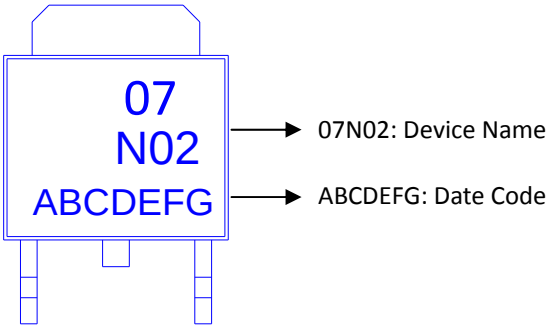
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

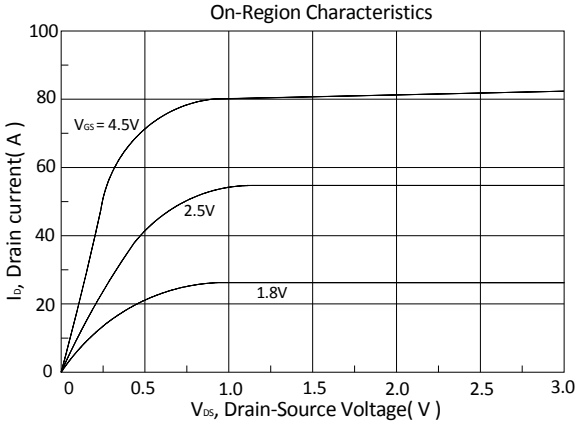
Ordering & Marking Information:

Device Name: LB07N02D for DPAK (TO-252)

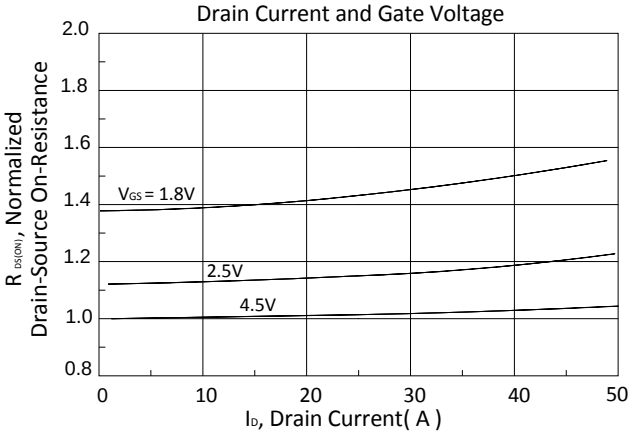


TYPICAL CHARACTERISTICS

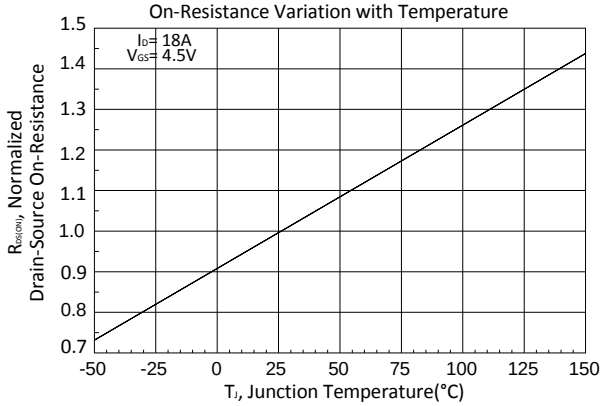
On-Region Characteristics



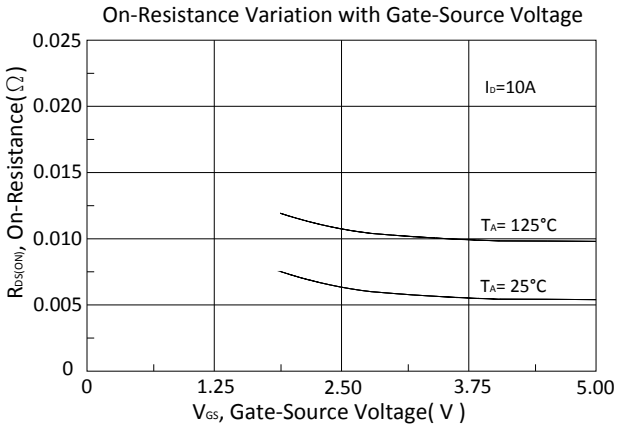
On-Resistance Variation with Drain Current and Gate Voltage



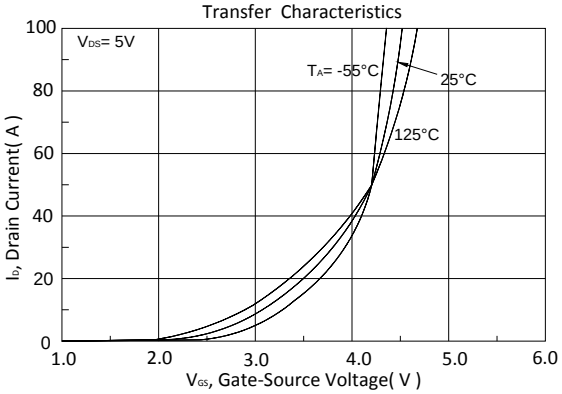
On-Resistance Variation with Temperature



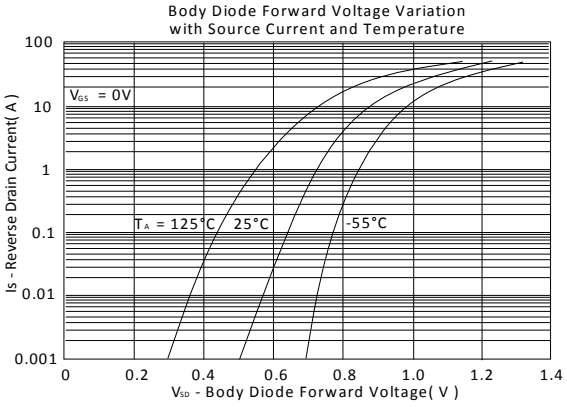
On-Resistance Variation with Gate-Source Voltage



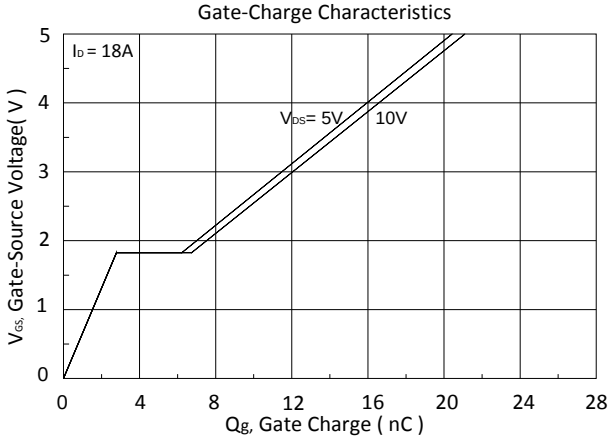
Transfer Characteristics



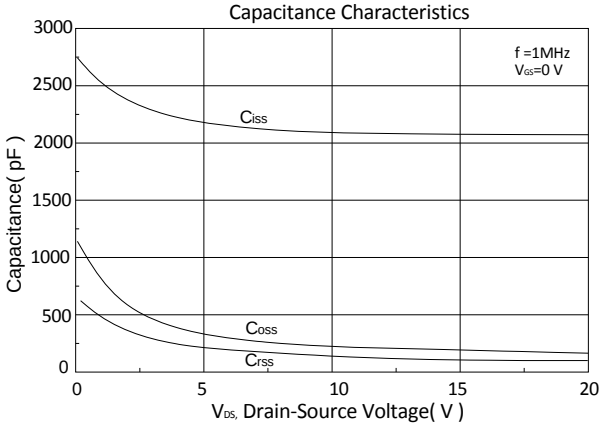
Body Diode Forward Voltage Variation with Source Current and Temperature



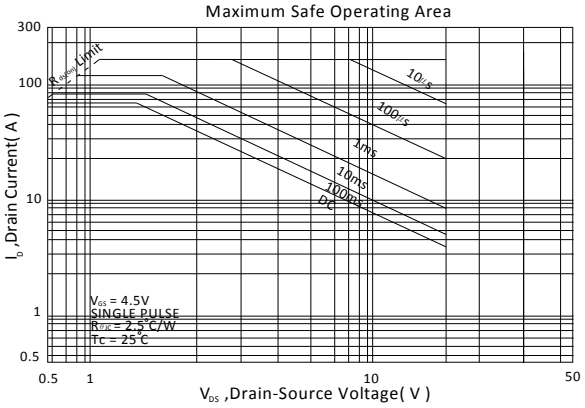
Gate-Charge Characteristics



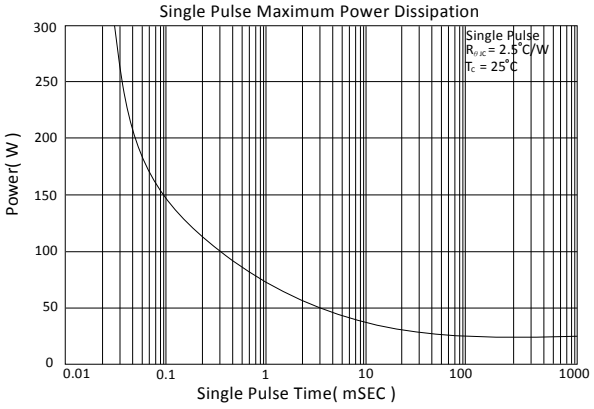
Capacitance Characteristics



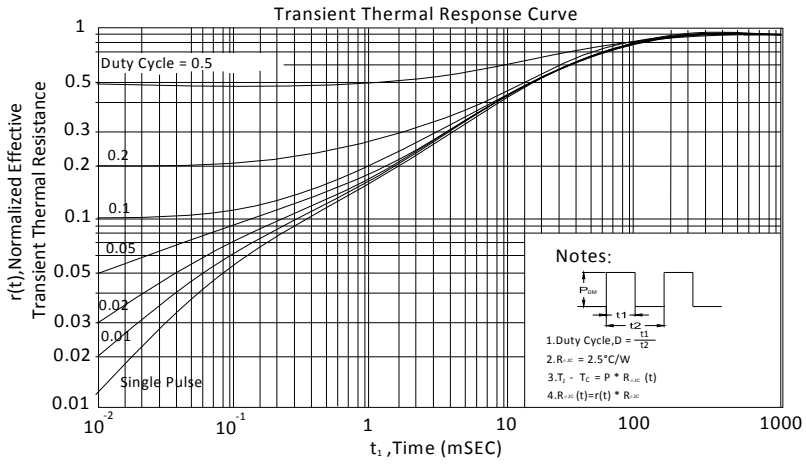
Maximum Safe Operating Area



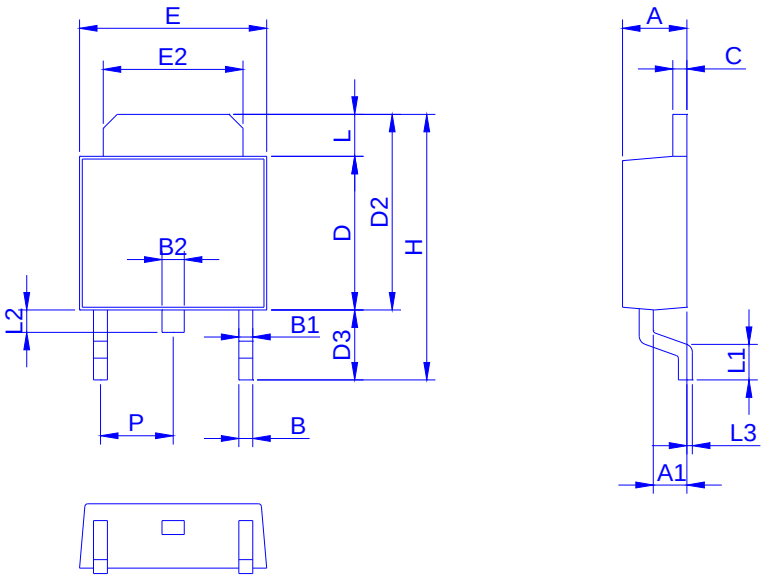
Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



Outline Drawing



Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	0.95	0.30	0.40	0.60	0.40	5.30	6.70	2.20	6.40	4.80	9.20	0.89	0.90	0.50	0.00	2.10
Max.	2.50	1.30	0.85	0.94	1.00	0.60	6.20	7.30	3.00	6.70	5.45	10.15	1.70	1.65	1.10	0.30	2.50

Footprint