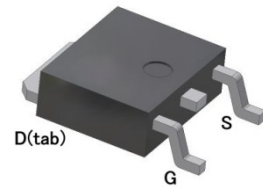
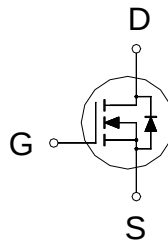


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	30V
R _{DS(on)} (MAX.)	4.0mΩ
I _D	90A



UIS, R_g 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _C = 25 °C	I _D	90	A
	T _C = 100 °C		55	
Pulsed Drain Current ¹		I _{DM}	180	
Avalanche Current		I _{AS}	53	mJ
Avalanche Energy	L = 0.1mH, I _D =53A, R _G =25 Ω	E _{AS}	140	
Repetitive Avalanche Energy ²	L = 0.05mH	E _{AR}	40	
Power Dissipation	T _C = 25 °C	P _D	69	W
	T _C = 100 °C		27	
Operating Junction & Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C

100% UIS testing in condition of V_D=15V, L=0.1mH, V_G=10V, I_L=40A, Rated V_{DS}=30V N-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}		1.8	°C / W
Junction-to-Ambient	R _{θJA}		75	

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

³75°C / W when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1	1.5	3	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 24V, V _{GS} = 0V			1	μA
		V _{DS} = 20V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	75			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 10V, I _D = 30A		3.2	4.0	mΩ
		V _{GS} = 4.5V, I _D = 24A		4.9	6.6	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 24A		25		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		3570		pF
Output Capacitance	C _{oss}			548		
Reverse Transfer Capacitance	C _{rss}			448		
Gate Resistance	R _g	V _{GS} = 15mV, V _{DS} = 0V, f = 1MHz		1.2		Ω
Total Gate Charge ^{1,2}	Q _g (V _{GS} =10V)	V _{DS} = 15V, V _{GS} = 10V, I _D = 30A		59		nC
	Q _g (V _{GS} =4.5V)			25		
Gate-Source Charge ^{1,2}	Q _{gs}			7.2		
Gate-Drain Charge ^{1,2}	Q _{gd}			12.7		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{DS} = 15V, I _D = 24A, V _{GS} = 10V, R _{GS} = 2.7Ω		18		nS
Rise Time ^{1,2}	t _r			12		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			55		
Fall Time ^{1,2}	t _f			15		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _c = 25 °C)						
Continuous Current	I _S				90	A
Pulsed Current ³	I _{SM}				180	
Forward Voltage ¹	V _{SD}	I _F = I _S , V _{GS} = 0V			1.3	V
Reverse Recovery Time	t _{rr}	I _F = I _S , dI _F /dt = 100A / μS		30		nS
Peak Reverse Recovery Current	I _{RM(REC)}			200		A
Reverse Recovery Charge	Q _{rr}			10		nC

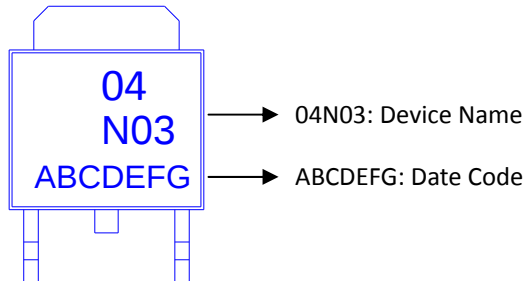
¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

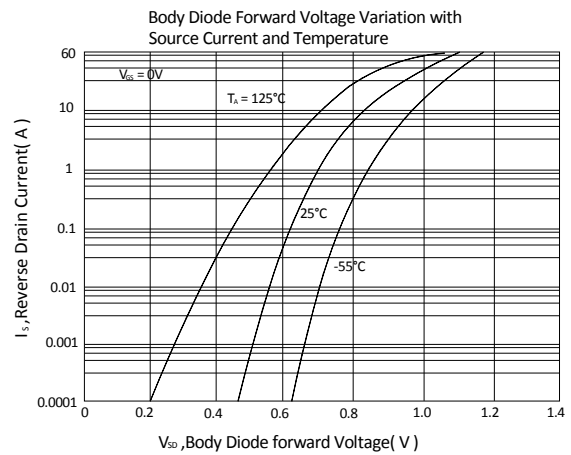
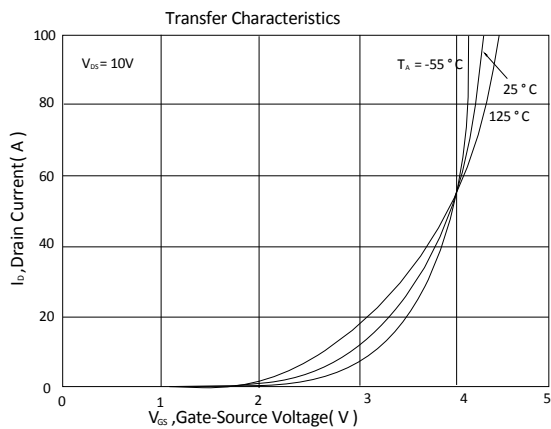
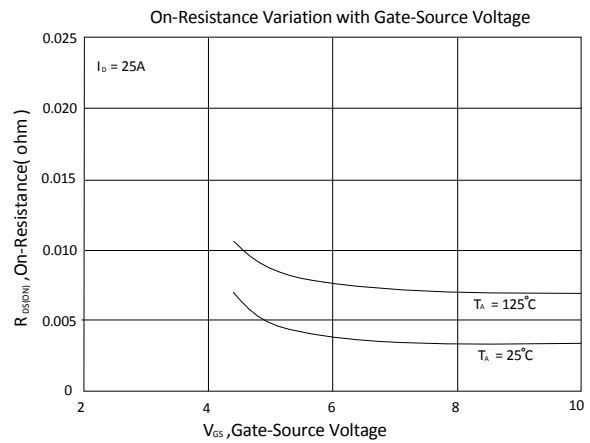
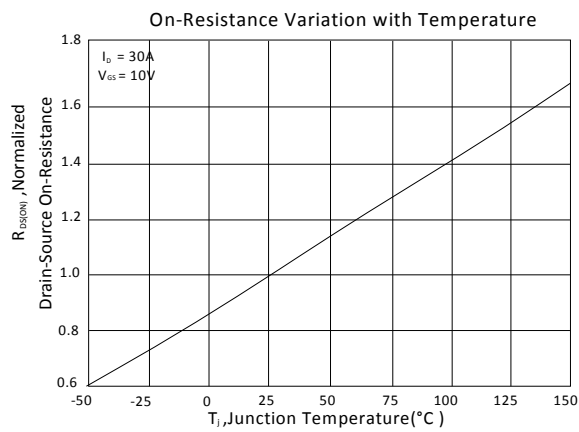
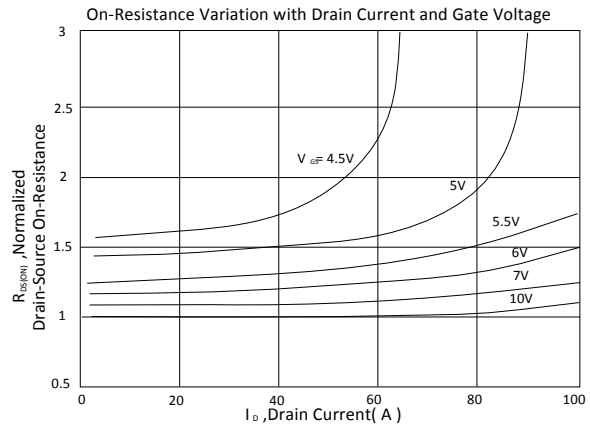
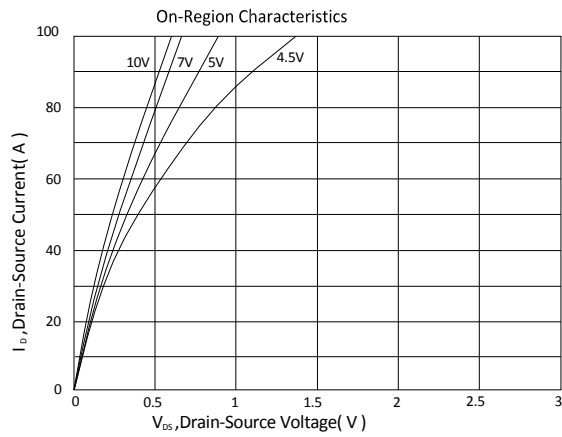
³Pulse width limited by maximum junction temperature.

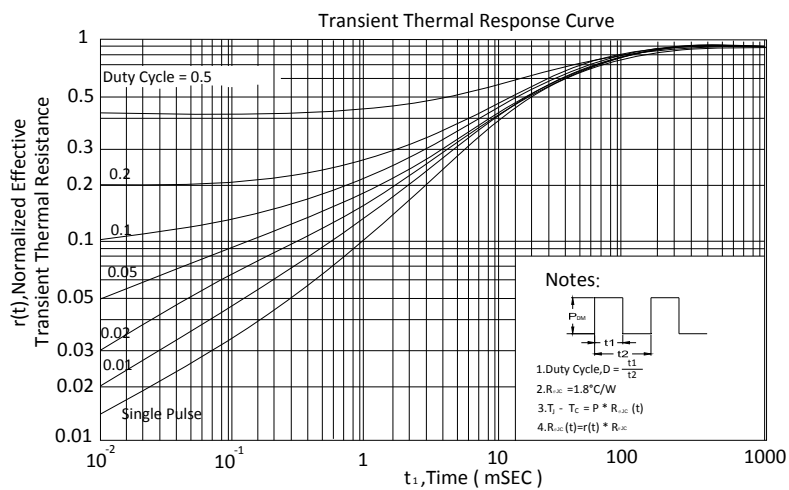
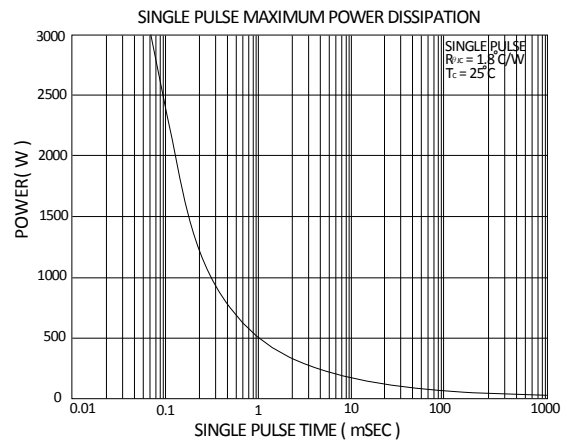
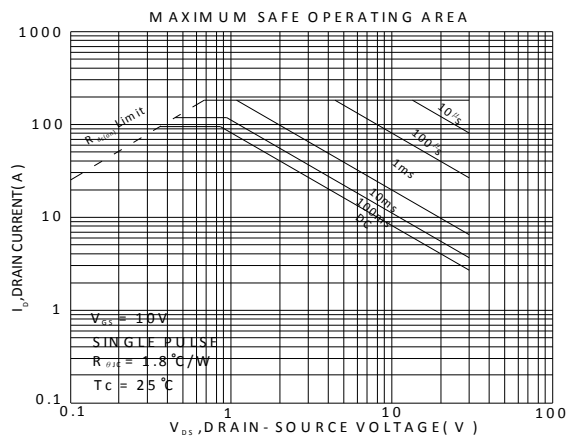
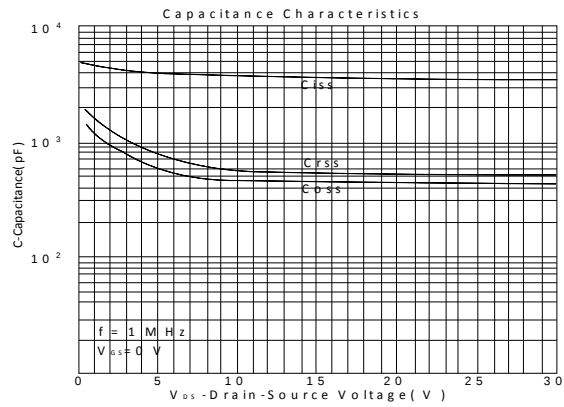
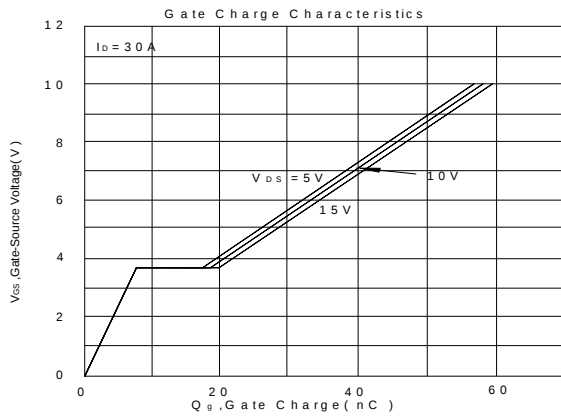
Ordering & Marking Information:

Device Name: LB04N03D for DPAK (TO-252)

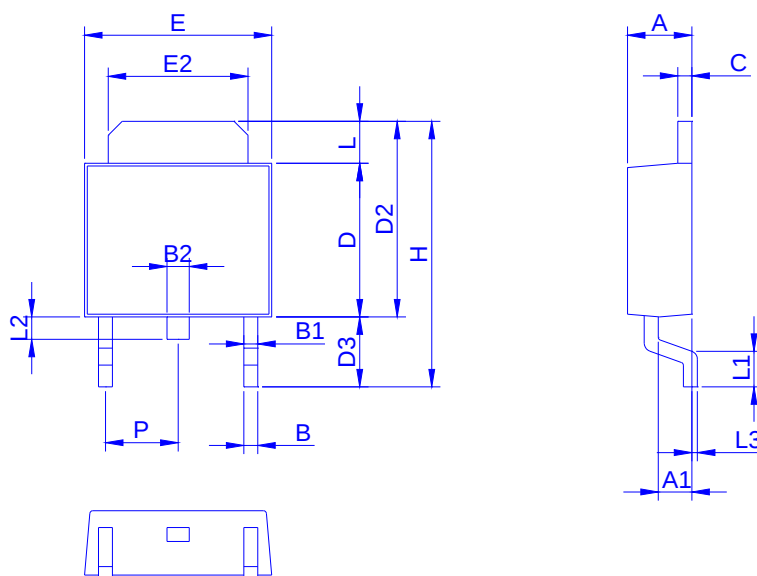


TYPICAL CHARACTERISTICS





Outline Drawing



Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	0.95	0.30	0.40	0.60	0.40	5.30	6.70	2.20	6.40	4.80	9.20	0.89	0.90	0.50	0.00	2.10
Max.	2.50	1.30	0.85	0.94	1.00	0.60	6.20	7.30	3.00	6.70	5.45	10.15	1.70	1.65	1.10	0.30	2.50

Footprint

