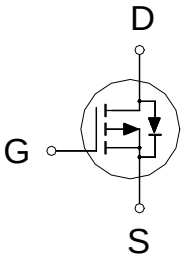
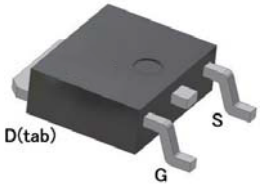
P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-20V
$R_{DSON\ (MAX.)}$	90mΩ
I_D	-10A





Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current	T_C = 25 °C	I_D	-10	A
	T_C = 100 °C		-6.5	
Pulsed Drain Current[1]		I_{DM}	-40	
Power Dissipation	T_C = 25 °C	P_D	25	W
	T_C = 100 °C		10	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		5	°C / W
Junction-to-Ambient	$R_{\theta JA}$		110	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

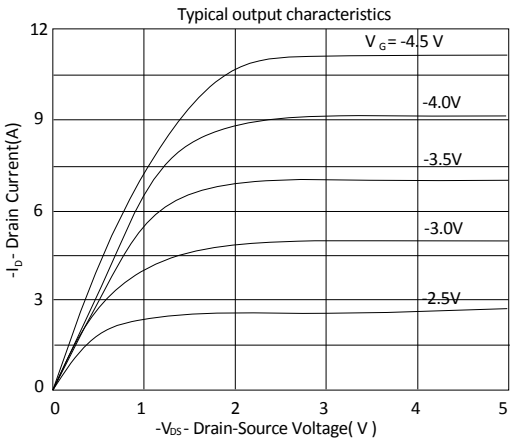
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-0.3	-0.75	-1.2	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -16V, V_{GS} = 0V			-1	μA
		V_{DS} = -16V, V_{GS} = 0V, T_J = 125 °C			-25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -4.5V	-10			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -4.5V, I_D = -6A		72	90	mΩ
		V_{GS} = -2.5V, I_D = -3A		120	150	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -5A		4.5		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -10V, f = 1MHz		382		pF
Output Capacitance	C_{oss}			70		
Reverse Transfer Capacitance	C_{rss}			60		
Total Gate Charge[1,2]	Q_g	V_{DS} = -10V, V_{GS} = -4.5V, I_D = -6A		7.2		nC
Gate-Source Charge[1,2]	Q_{gs}			1.2		
Gate-Drain Charge[1,2]	Q_{gd}			2.3		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = -10V, I_D = -1A, V_{GS} = -4.5V, R_{GS} = 6Ω		10		nS
Rise Time[1,2]	t_r			20		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			15		
Fall Time[1,2]	t_f			12		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				-10	A
Pulsed Current[3]	I_{SM}				-40	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			1.3	V

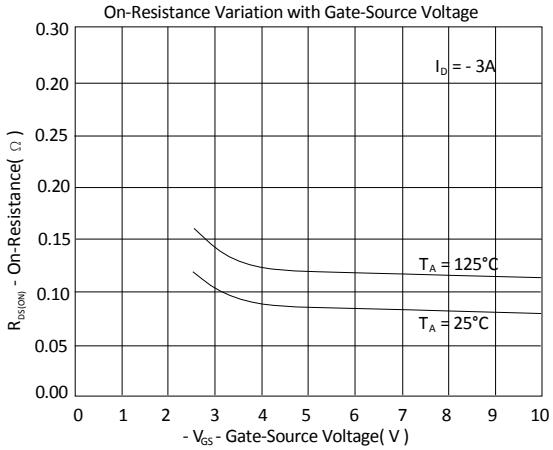
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

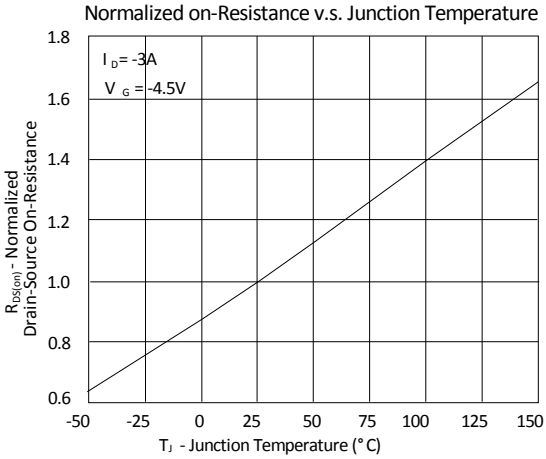
[2]Independent of operating temperature.

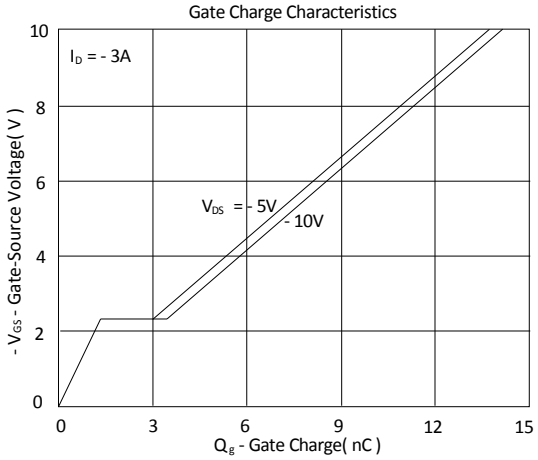
[3]Pulse width limited by maximum junction temperature.

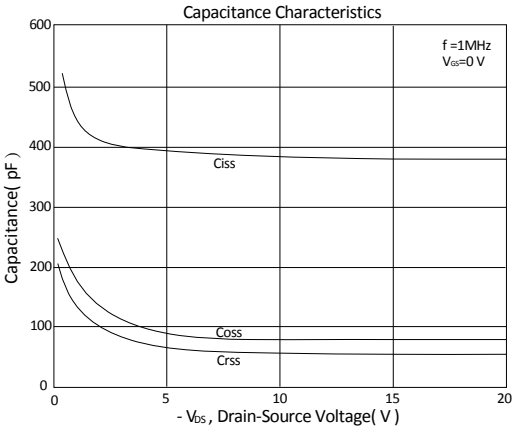
TYPICAL CHARACTERISTICS

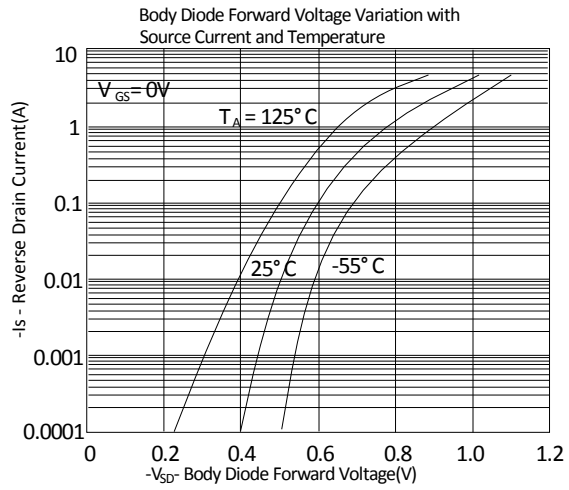




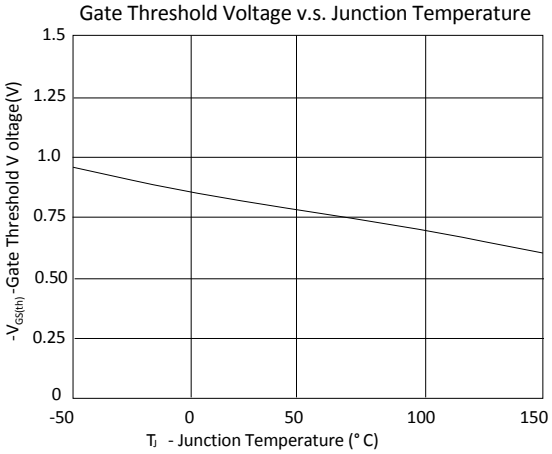




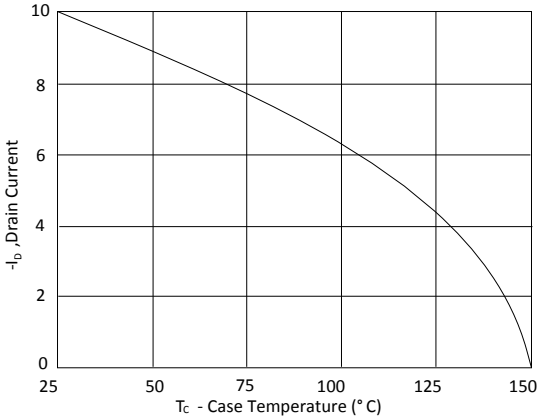




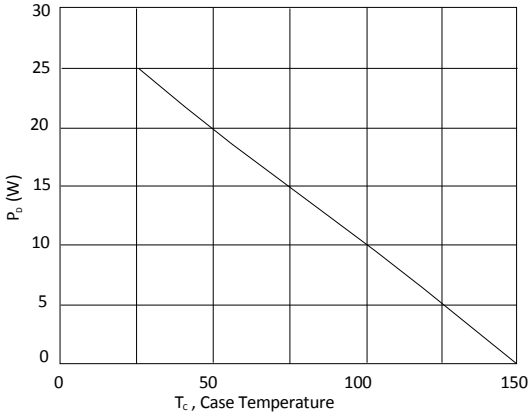
Gate Threshold Voltage v.s. Junction Temperature



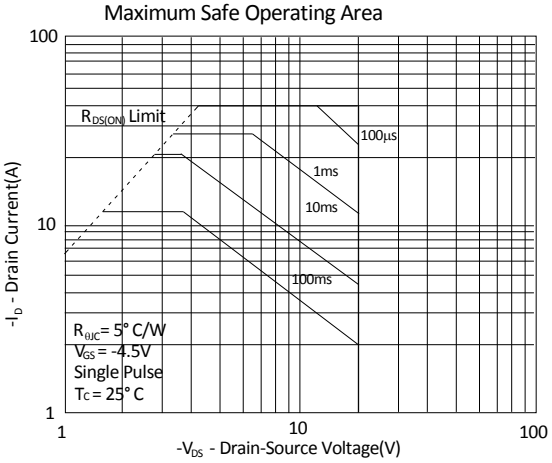
Maximum Drain Current v.s. Case Temperature



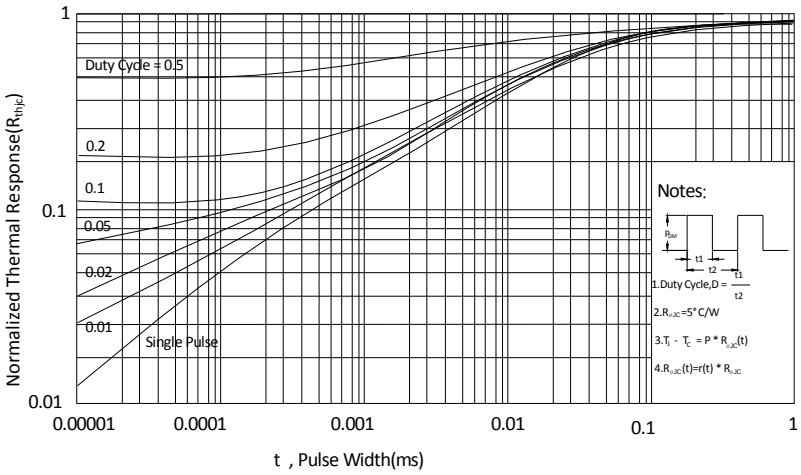
Typical Power Dissipation



Maximum Safe Operating Area

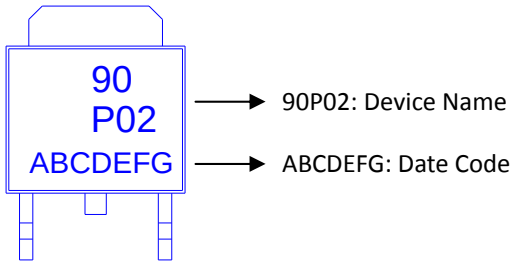


Effective Transient Thermal Impedance

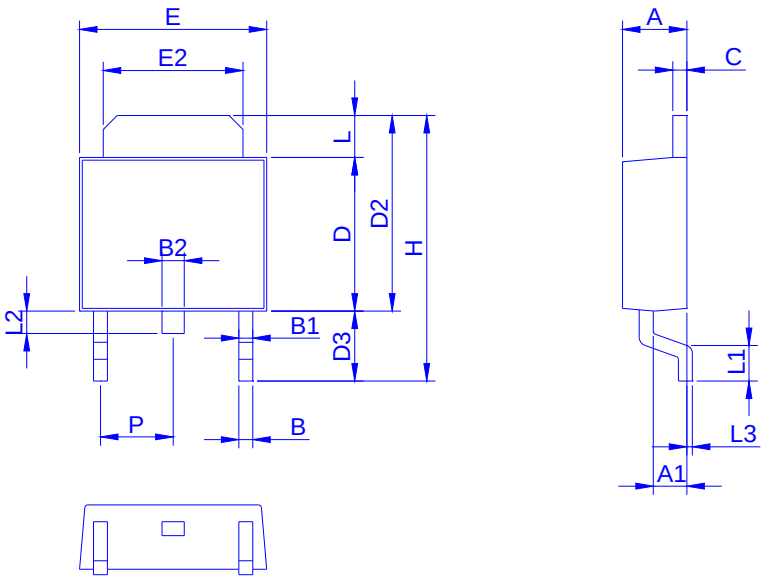


Ordering & Marking Information:

Device Name: LB90P02D for DPAK (TO-252)



Outline Drawing



Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	0.95	0.30	0.40	0.60	0.40	5.30	6.70	2.20	6.40	4.80	9.20	0.89	0.90	0.50	0.00	2.10
Max.	2.50	1.30	0.85	0.94	1.00	0.60	6.20	7.30	3.00	6.70	5.45	10.15	1.70	1.65	1.10	0.30	2.50

Footprint