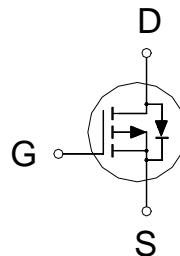


**P-Channel Logic Level Enhancement Mode Field Effect Transistor**
**Product Summary:**

$BV_{DSS}$	-20V
$R_{DS(on)}$ (MAX.)	44mΩ
$I_D$	-4A


**Pb-Free Lead Plating & Halogen Free**

**ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$  Unless Otherwise Noted)**

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNIT
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Continuous Drain Current	$I_D$	-4	A
		-3	
Pulsed Drain Current <sup>1</sup>	$I_{DM}$	-16	
Power Dissipation	$P_D$	1.04	W
		0.66	
Operating Junction & Storage Temperature Range	$T_j, T_{stg}$	-55 to 150	°C

**THERMAL RESISTANCE RATINGS**

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Ambient <sup>3</sup>	$R_{\theta JA} (T \leq 10\text{sec})$		83	°C / W
	$R_{\theta JA} (\text{Steady State})$		120	

<sup>1</sup>Pulse width limited by maximum junction temperature.

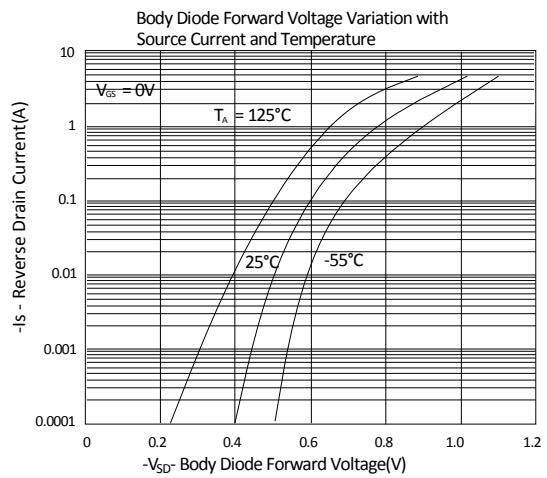
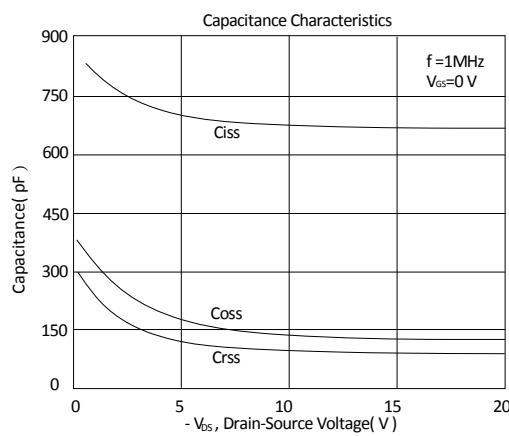
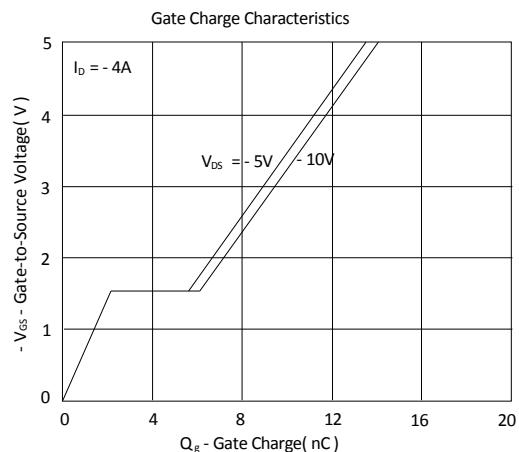
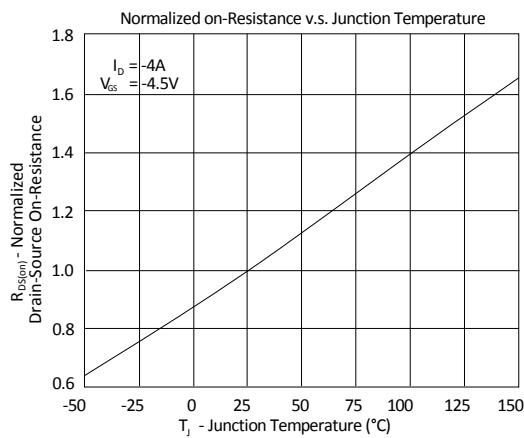
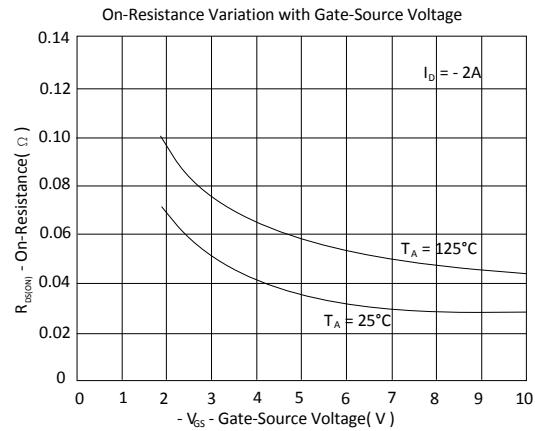
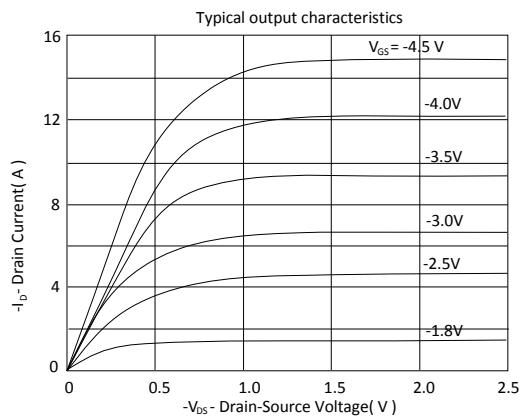
<sup>2</sup>Duty cycle  $\leq 1\%$ 
<sup>3</sup>The device mounted on a 1 in<sup>2</sup> pad of 2 oz copper.

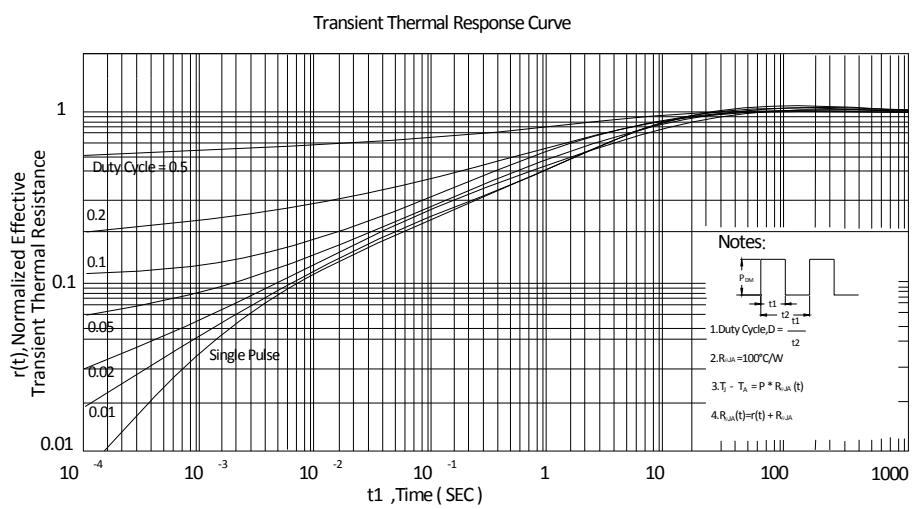
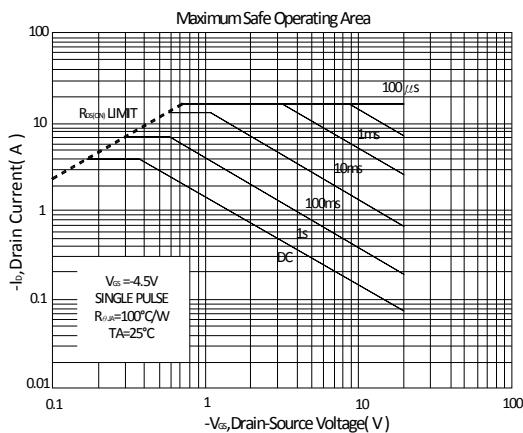
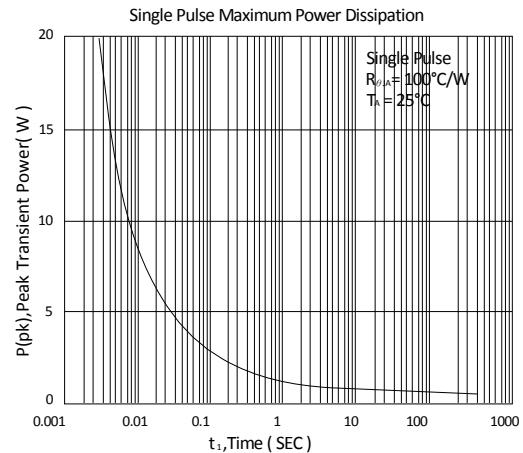
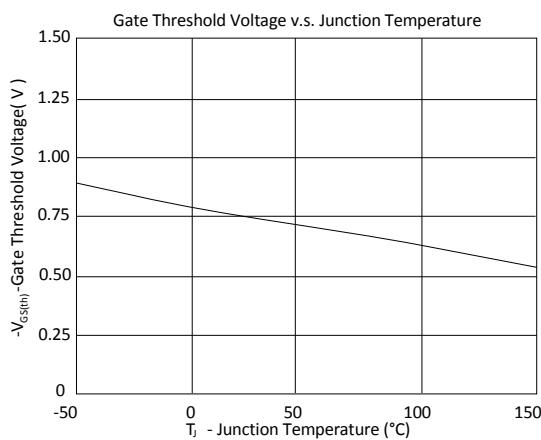
**ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Noted)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	$V_{(\text{BR})DSS}$	$V_{GS} = 0V, I_D = -250\mu\text{A}$	-20			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-0.3	-0.75	-1.0	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 12V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -16V, V_{GS} = 0V$			-1	$\mu\text{A}$
		$V_{DS} = -16V, V_{GS} = 0V, T_J = 125^\circ\text{C}$			-10	
On-State Drain Current <sup>1</sup>	$I_{D(\text{ON})}$	$V_{DS} = -5V, V_{GS} = -4.5V$	-4			A
Drain-Source On-State Resistance <sup>1</sup>	$R_{DS(\text{ON})}$	$V_{GS} = -4.5V, I_D = -4A$		37	44	$\text{m}\Omega$
		$V_{GS} = -2.5V, I_D = -3A$		55	70	
		$V_{GS} = -1.8V, I_D = -1A$		65	90	
Forward Transconductance <sup>1</sup>	$g_{fs}$	$V_{DS} = -5V, I_D = -4A$		14		S
<b>DYNAMIC</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V, V_{DS} = -10V, f = 1\text{MHz}$		679		$\text{pF}$
Output Capacitance	$C_{oss}$			124		
Reverse Transfer Capacitance	$C_{rss}$			106		
Total Gate Charge <sup>1,2</sup>	$Q_g$	$V_{DS} = -10V, V_{GS} = -4.5V, I_D = -4A$		12.8		$\text{nC}$
Gate-Source Charge <sup>1,2</sup>	$Q_{gs}$			2.2		
Gate-Drain Charge <sup>1,2</sup>	$Q_{gd}$			4.1		
Turn-On Delay Time <sup>1,2</sup>	$t_{d(\text{on})}$	$V_{DS} = -10V, I_D = -1A, V_{GS} = -4.5V, R_{GS} = 6\Omega$		10		$\text{nS}$
Rise Time <sup>1,2</sup>	$t_r$			18		
Turn-Off Delay Time <sup>1,2</sup>	$t_{d(\text{off})}$			32		
Fall Time <sup>1,2</sup>	$t_f$			22		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (<math>T_C = 25^\circ\text{C}</math>)</b>						
Continuous Current	$I_S$				-3	$\text{A}$
Pulsed Current <sup>3</sup>	$I_{SM}$				-12	
Forward Voltage <sup>1</sup>	$V_{SD}$	$I_F = I_S, V_{GS} = 0V$			-1.2	V

<sup>1</sup>Pulse test : Pulse Width  $\leq 300 \mu\text{sec}$ , Duty Cycle  $\leq 2\%$ .<sup>2</sup>Independent of operating temperature.<sup>3</sup>Pulse width limited by maximum junction temperature.

## TYPICAL CHARACTERISTICS

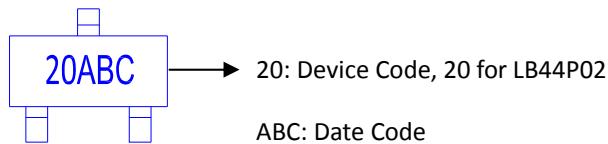




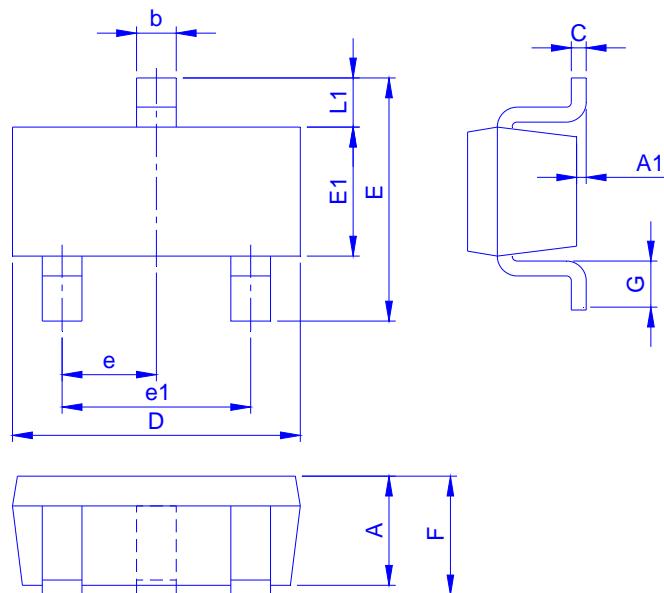
## Ordering & Marking

Information:

Device Name: LB44P02QS for SOT-23



## Outline Drawing



## Dimension in mm

Dimension	A	A1	b	C	D	E	E1	e	e1	F	G	L1
Min.	0.70	0	0.3	0.08	2.80	2.25	1.2	0.90		0.80	0.3	0.50
Typ.					2.90			0.95	1.9			
Max.	1.15	0.1	0.5	0.20	3.02	3.00	1.7	1.00		1.25	0.6	0.75

## Footprint

