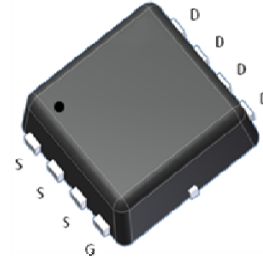
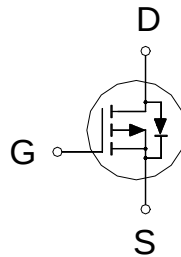


P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-20V
$R_{DS(on)} (MAX.)$	44m Ω
I_D	-9.5A



Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^{\circ}\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 12	V
Continuous Drain Current	$T_A = 25\text{ }^{\circ}\text{C}$	I_D	-9.5	A
	$T_A = 70\text{ }^{\circ}\text{C}$		-7.2	
Pulsed Drain Current ¹		I_{DM}	-38	
Power Dissipation	$T_A = 25\text{ }^{\circ}\text{C}$	P_D	2.5	W
	$T_A = 70\text{ }^{\circ}\text{C}$		1.25	
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150	$^{\circ}\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		6	$^{\circ}\text{C} / \text{W}$
Junction-to-Ambient ³	$R_{\theta JA}$		50	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³50 $^{\circ}\text{C} / \text{W}$ when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_A = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-20			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-0.3	-0.75	-1.2	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -16V, V _{GS} = 0V			-1	μA
		V _{DS} = -16V, V _{GS} = 0V, T _J = 125 °C			-10	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = -5V, V _{GS} = -4.5V	-4			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = -4.5V, I _D = -5A		37	44	mΩ
		V _{GS} = -2.5V, I _D = -4A		55	70	
		V _{GS} = -1.8V, I _D = -1A		65	90	
Forward Transconductance ¹	g _{fs}	V _{DS} = -5V, I _D = -4A		14		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = -10V, f = 1MHz		679		pF
Output Capacitance	C _{oss}			124		
Reverse Transfer Capacitance	C _{rss}			106		
Total Gate Charge ^{1,2}	Q _g	V _{DS} = -10V, V _{GS} = -4.5V, I _D = -4A		12.8		nC
Gate-Source Charge ^{1,2}	Q _{gs}			2.2		
Gate-Drain Charge ^{1,2}	Q _{gd}			4.1		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{DS} = -10V, I _D = -1A, V _{GS} = -4.5V, R _{GS} = 6Ω		10		nS
Rise Time ^{1,2}	t _r			18		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			32		
Fall Time ^{1,2}	t _f			22		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _C = 25 °C)						
Continuous Current	I _S				-3	A
Pulsed Current ³	I _{SM}				-12	
Forward Voltage ¹	V _{SD}	I _F = I _S , V _{GS} = 0V			-1.2	V

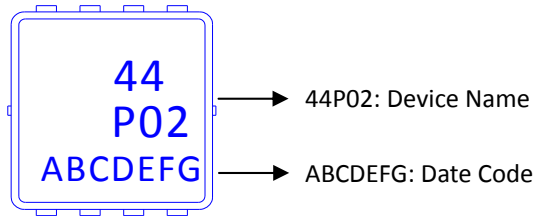
¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

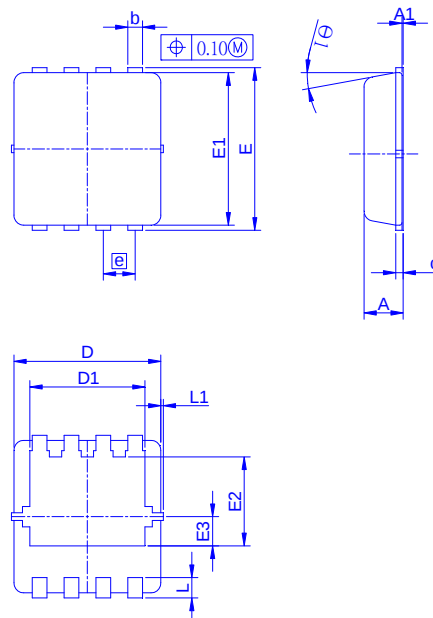
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: LB44P02B for EDFN 3 x 3



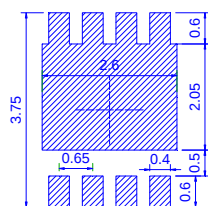
Outline Drawing



Dimension in mm

Dimension	A	A1	b	c	D	D1	E	E1	E2	E3	e	L	L1	Θ1
Min.	0.70	0	0.24	0.10	2.95	2.25	3.15	2.95	1.65			0.30		0°
Typ.	0.80		0.30	0.152	3.00	2.35	3.20	3.00	1.75	0.575	0.65	0.40	0.13	10°
Max.	0.90	0.05	0.37	0.25	3.15	2.45	3.40	3.15	1.96			0.50		12°

Recommended minimum pads



TYPICAL CHARACTERISTICS

