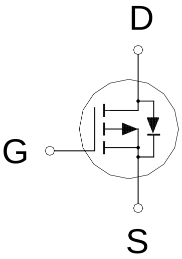
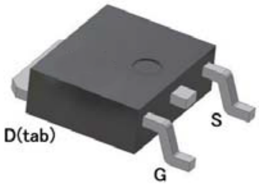
P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-30V
$R_{DSON\ (MAX.)}$	30mΩ
I_D	-22A





UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	-22	A
	T_C = 100 °C		-18	
Pulsed Drain Current[1]		I_{DM}	-60	
Avalanche Current		I_{AS}	-12	
Avalanche Energy	L = 0.1mH, ID=-12A, RG=25Ω	E_{AS}	7.2	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	E_{AR}	3.6	
Power Dissipation	T_C = 25 °C	P_D	33	W
	T_C = 100 °C		13	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		3.75	°C / W
Junction-to-Ambient	$R_{\theta JA}$		80	

[1] Pulse width limited by maximum junction temperature.

[2] Duty cycle $\leq$ 1%

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250µA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250µA	-1.0	-1.5	-3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24V, V_{GS} = 0V			-1	µA
		V_{DS} = -20V, V_{GS} = 0V, T_J = 125 °C			-25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -10V	-22			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -10V, I_D = -20A		26	30	mΩ
		V_{GS} = -4.5V, I_D = -7A		41	51	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -15A		12		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -15V, f = 1MHz		910		pF
Output Capacitance	C_{oss}			143		
Reverse Transfer Capacitance	C_{rss}			108		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz		4.0		Ω
Total Gate Charge[1,2]	Q_g	V_{DS} = -15V, V_{GS} = -10V, I_D = -15A		13.3		nC
Gate-Source Charge[1,2]	Q_{gs}			2.1		
Gate-Drain Charge[1,2]	Q_{gd}			3.2		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = -10V, I_D = -1A, V_{GS} = -10V, R_{GS} = 6Ω		12		nS
Rise Time[1,2]	t_r			18		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			38		
Fall Time[1,2]	t_f			22		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				-15	A
Pulsed Current[3]	I_{SM}				-60	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			-1.3	V
Reverse Recovery Time	t_{rr}	I_F = -5A, dI_F/dt = 100A / µS		55		nS
Reverse Recovery Charge	Q_{rr}			2.2		nC

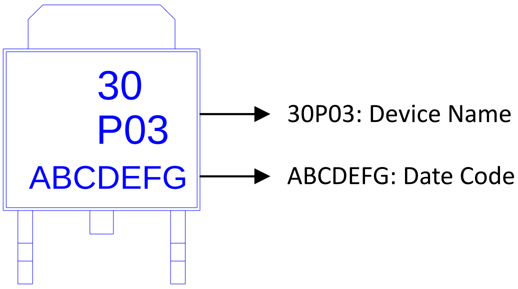
[1] Pulse test : Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.

[2] Independent of operating temperature.

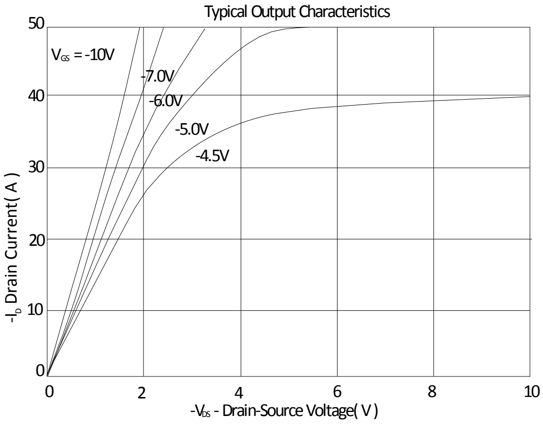
[3] Pulse width limited by maximum junction temperature.

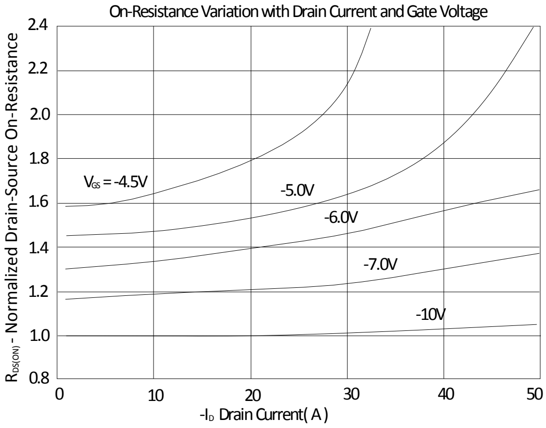
Ordering & Marking Information:

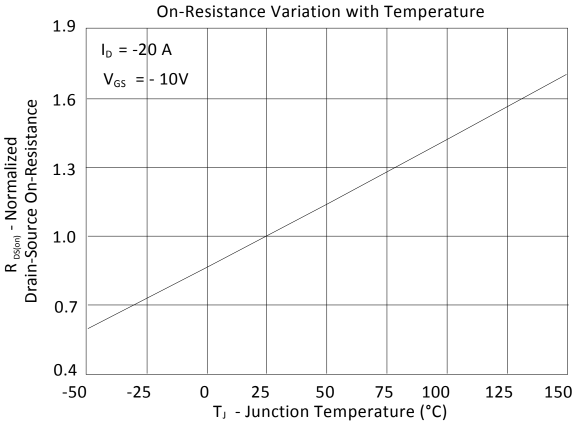
Device Name: LB30P03D for DPAK (TO-252)

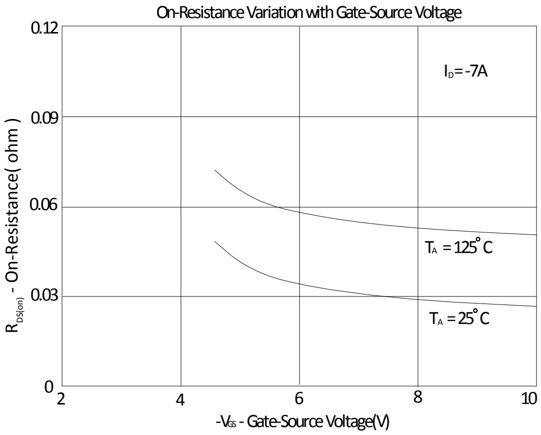


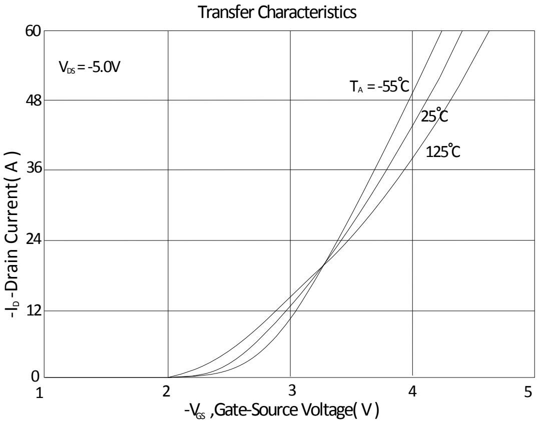
TYPICAL CHARACTERISTICS

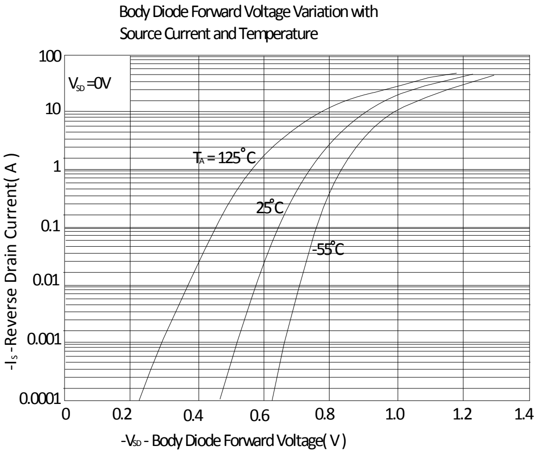




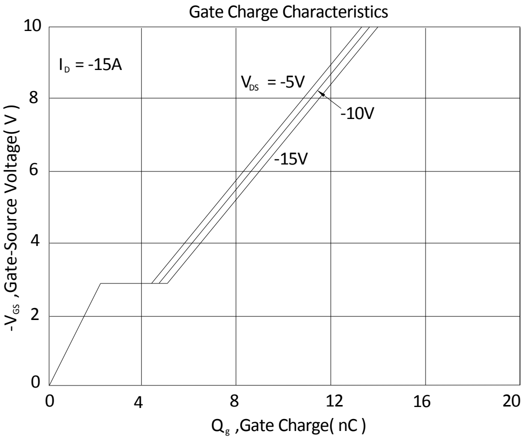




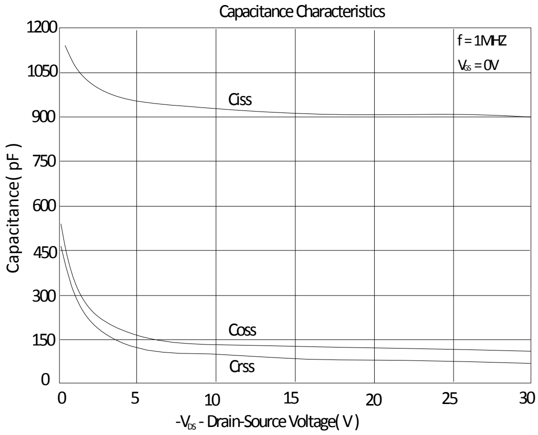




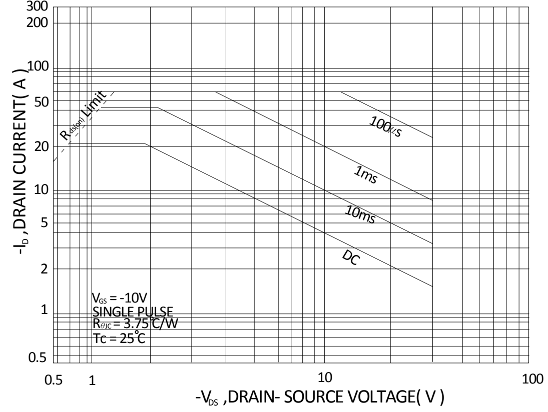
Gate Charge Characteristics



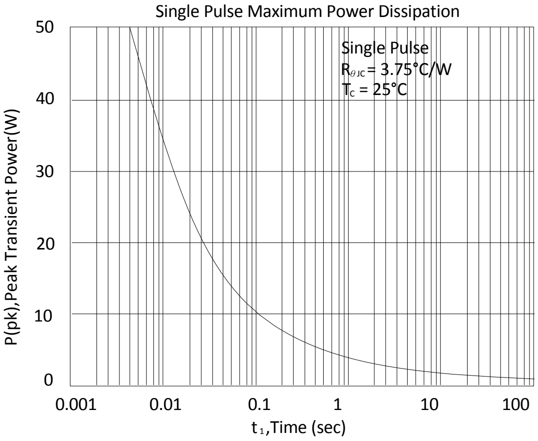
Capacitance Characteristics



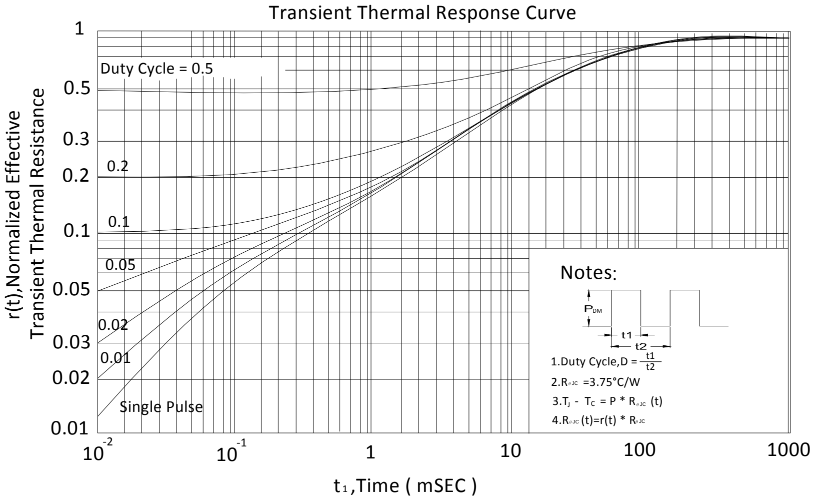
MAXIMUM SAFE OPERATING AREA



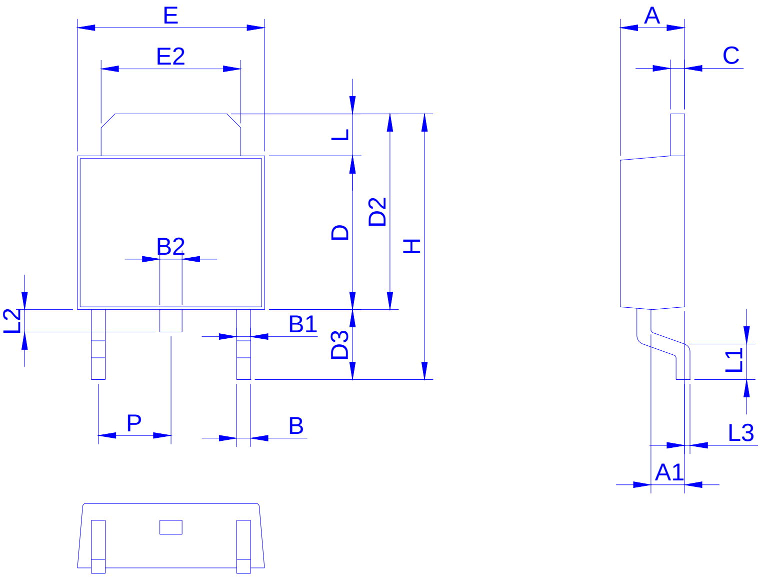
Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



Outline Drawing



Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	0.95	0.30	0.40	0.60	0.40	5.30	6.70	2.20	6.40	4.80	9.20	0.89	0.90	0.50	0.00	2.10
Max.	2.50	1.30	0.85	0.94	1.00	0.60	6.20	7.30	3.00	6.70	5.45	10.15	1.70	1.65	1.10	0.30	2.50

Footprint