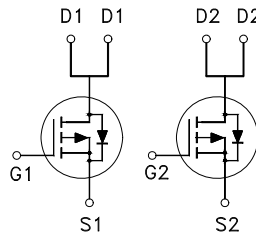


Dual P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-30V
$R_{DS(on)} (MAX.)$	35m Ω
I_D	-6.5A



Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_A = 25\text{ }^{\circ}\text{C}$	I_D	-6.5	A
	$T_A = 100\text{ }^{\circ}\text{C}$		-4.9	
Pulsed Drain Current ¹		I_{DM}	-26	
Power Dissipation	$T_A = 25\text{ }^{\circ}\text{C}$	P_D	2	W
	$T_A = 100\text{ }^{\circ}\text{C}$		1.08	
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150	$^{\circ}\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		25	$^{\circ}\text{C} / \text{W}$
Junction-to-Ambient ³	$R_{\theta JA}$		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³62.5 $^{\circ}\text{C} / \text{W}$ when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1.0	-1.5	-3.0	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -24V, V_{GS} = 0V$			-1	μA
		$V_{DS} = -20V, V_{GS} = 0V, T_J = 125\text{ }^{\circ}C$			-10	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = -5V, V_{GS} = -10V$	-6.5			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = -10V, I_D = -6.5A$		30	35	m Ω
		$V_{GS} = -5V, I_D = -4.5A$		43	55	
Forward Transconductance ¹	g_{fs}	$V_{DS} = -5V, I_D = -6.5A$		12		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -15V, f = 1MHz$		910		pF
Output Capacitance	C_{oss}			143		
Reverse Transfer Capacitance	C_{rss}			108		
Gate Resistance	R_g	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		4.0		Ω
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = -15V, V_{GS} = -10V,$ $I_D = -6.5A$		13.3		nC
Gate-Source Charge ^{1,2}	Q_{gs}			2.1		
Gate-Drain Charge ^{1,2}	Q_{gd}			3.2		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = -15V,$ $I_D = -1A, V_{GS} = -10V, R_{GS} = 6\Omega$		12		nS
Rise Time ^{1,2}	t_r			18		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			38		
Fall Time ^{1,2}	t_f			22		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _C = 25 °C)						
Continuous Current	I_S				-2.3	A
Pulsed Current ³	I_{SM}				-9.2	
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			-1.3	V
Reverse Recovery Time	t_{rr}	$I_F = I_S, dI_F/dt = 100A / \mu S$		55		nS
Reverse Recovery Charge	Q_{rr}			3		nC

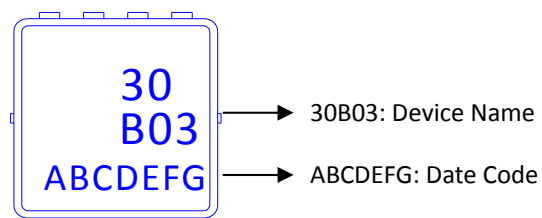
¹Pulse test : Pulse Width $\leq 300\text{ }\mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

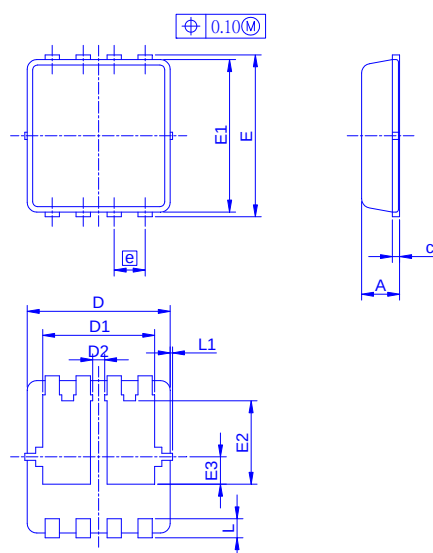
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: LB30P03BD for EDFN 3 x 3



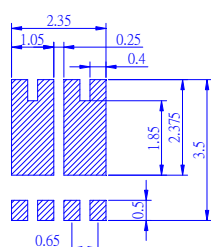
Outline Drawing



Dimension in mm

Dimension	A	A1	b	c	D	D1	D2	E	E1	E2	E3	e	L	L1	θ1
Min.	0.70	0	0.24	0.10	2.95	2.25		3.15	2.95	1.65			0.30	0	0°
Typ.	0.80		0.30	0.152	3.00	2.35	0.225	3.20	3.00	1.75	0.575	0.65	0.40		10°
Max.	0.90	0.05	0.35	0.25	3.05	2.45		3.25	3.05	1.85			0.50	0.10	12°

Recommended minimum pads



TYPICAL CHARACTERISTICS

