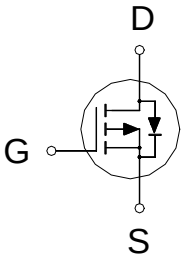
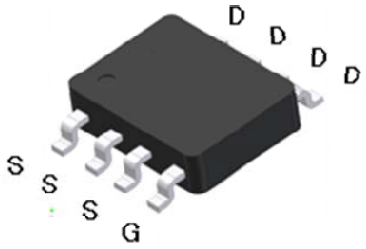
P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-30V
$R_{DSON\ (MAX.)}$	14mΩ
I_D	-12A





UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±25	V
Continuous Drain Current	T_A = 25 °C	I_D	-12	A
	T_A = 100 °C		-9	
Pulsed Drain Current[1]		I_{DM}	-48	
Avalanche Current		I_{AS}	-20	
Avalanche Energy	L = 0.1mH, I_D=-20A, R_G=25Ω	E_{AS}	20	mJ
Power Dissipation	T_A = 25 °C	P_D	2.5	W
	T_A = 100 °C		1	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

100% UIS testing in condition of V_D=-15V, L=0.1mH, V_G=-10V, I_L=-12A, Rated V_{DS}=-30V P-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		25	°C / W
Junction-to-Ambient[3]	$R_{\theta JA}$		50	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

[3]50°C / W when mounted on a 1 in^2 pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1	-1.5	-3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
		V_{DS} = 0V, V_{GS} = ±25V			±500	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24V, V_{GS} = 0V			-1	μA
		V_{DS} = -20V, V_{GS} = 0V, T_J = 125 °C			-10	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -10V	-12			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -10V, I_D = -12A		12	14	mΩ
		V_{GS} = -4.5V, I_D = -9A		17	21	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -12A		28		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -15V, f = 1MHz		2270		pF
Output Capacitance	C_{oss}			342		
Reverse Transfer Capacitance	C_{rss}			300		
Total Gate Charge[1,2]	Q_g(V_{GS}=-10V)	V_{DS} = -15V, V_{GS} = -10V, I_D = -10A		39.3		nC
	Q_g(V_{GS}=-4.5V)			16		
Gate-Source Charge[1,2]	Q_{gs}			4.9		
Gate-Drain Charge[1,2]	Q_{gd}			7.5		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = -15V, I_D = -1A, V_{GS} = -10V, R_{GS} = 2.7Ω		20		nS
Rise Time[1,2]	t_r			12		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			55		
Fall Time[1,2]	t_f			15		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				-3.6	A
Pulsed Current[3]	I_{SM}				-14.4	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			-1.2	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100A / μS		52		nS
Reverse Recovery Charge	Q_{rr}			60		nC

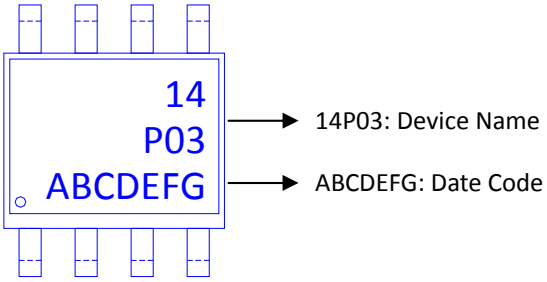
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

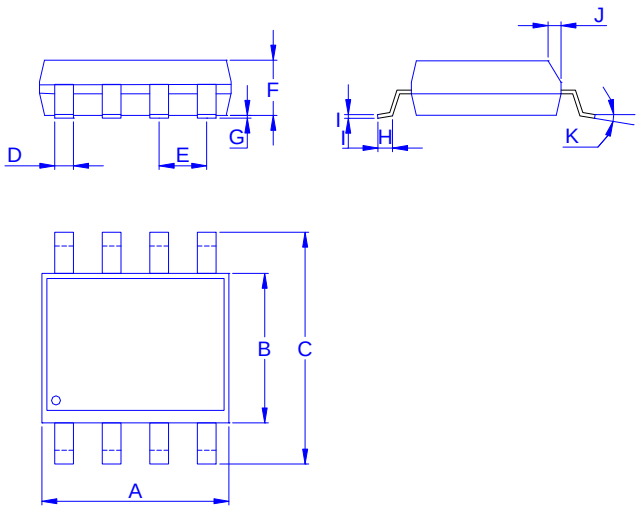
[3]Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: LB14P03H for SOP-8



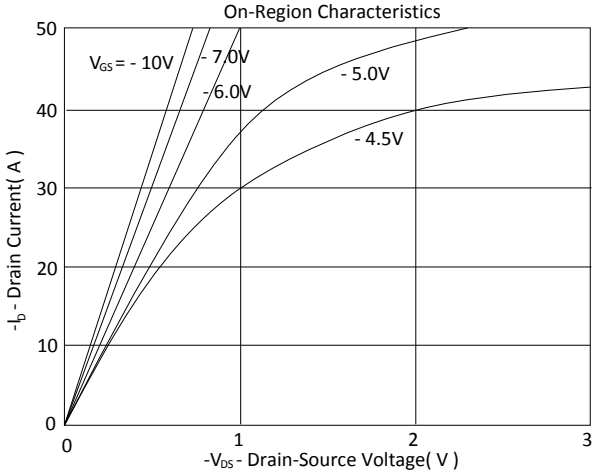
Outline Drawing



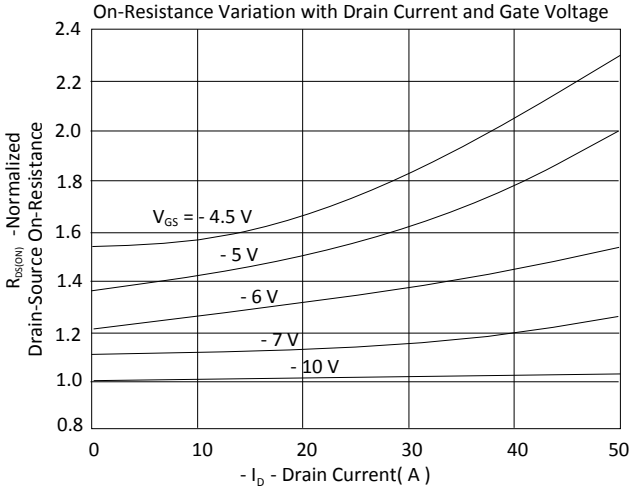
Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
in.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°

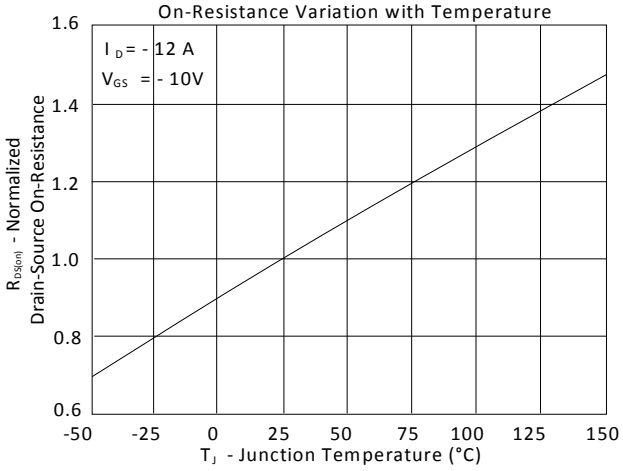
On-Region Characteristics



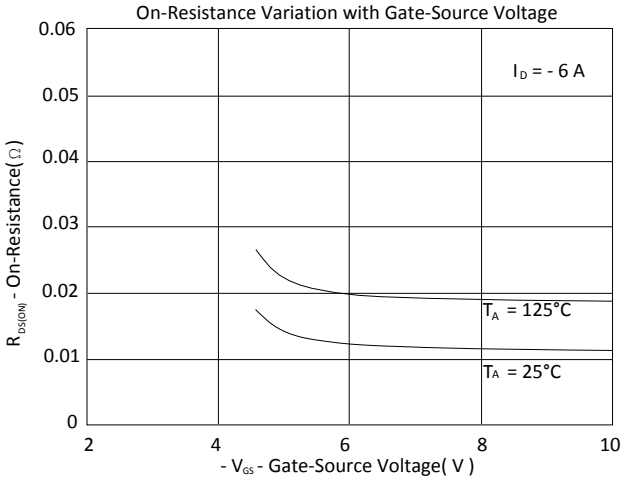
On-Resistance Variation with Drain Current and Gate Voltage



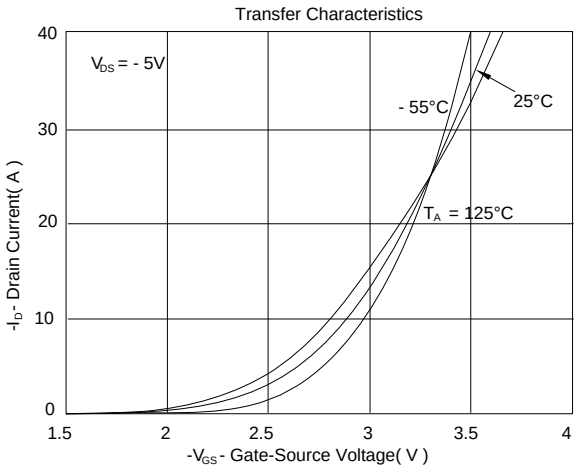
On-Resistance Variation with Temperature



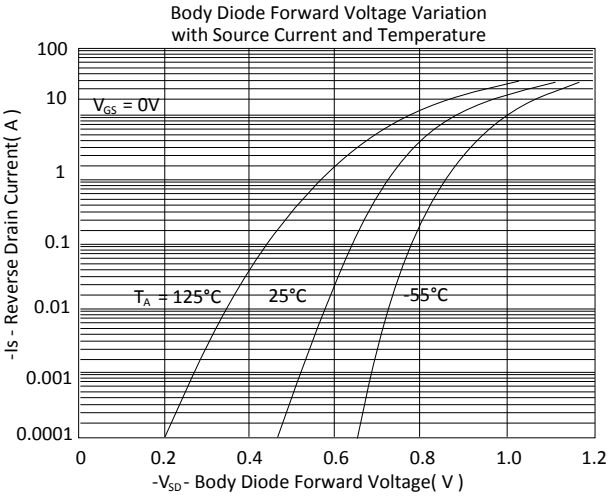
On-Resistance Variation with Gate-Source Voltage



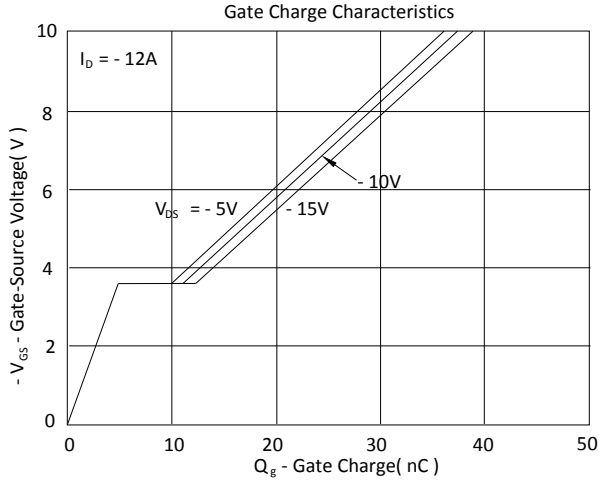
Transfer Characteristics



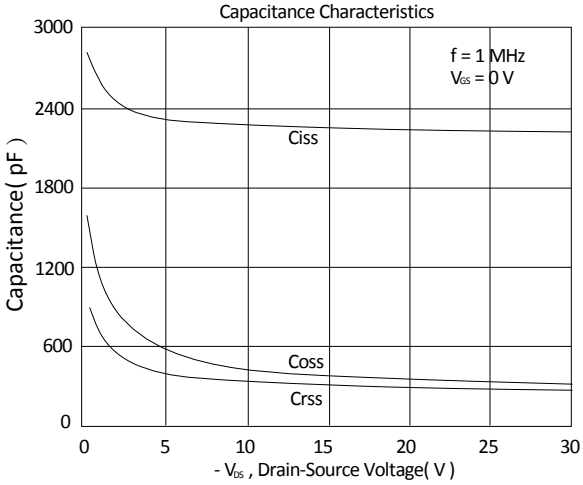
Body Diode Forward Voltage Variation
with Source Current and Temperature



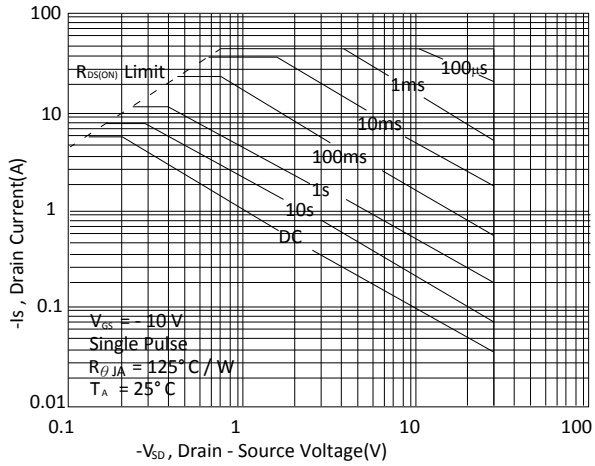
Gate Charge Characteristics



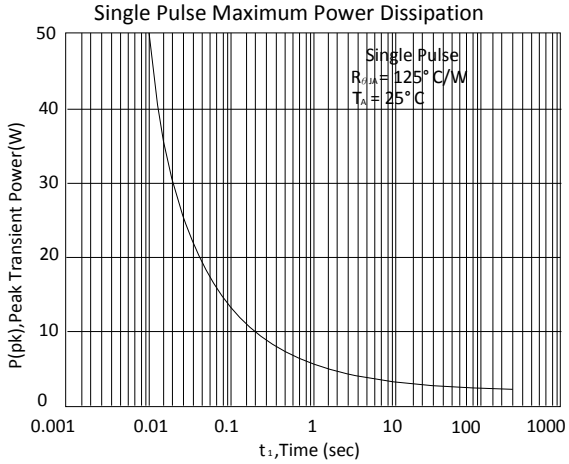
Capacitance Characteristics



Maximum Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve