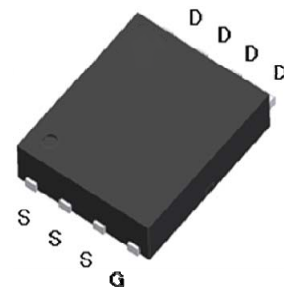


P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	-30V
R _{DS(on)} (MAX.)	12mΩ
I _D	-50A



UIS, R_g 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _C = 25 °C	I _D	-50	A
	T _C = 100 °C		-36	
Pulsed Drain Current ¹		I _{DM}	-120	
Avalanche Current		I _{AS}	-20	
Avalanche Energy	L = 0.1mH, I _D = -20A, R _G = 25 Ω	E _{AS}	20	mJ
Power Dissipation	T _C = 25 °C	P _D	50	W
	T _C = 100 °C		20	
Operating Junction & Storage Temperature Range		T _j , T _{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}		2.5	°C / W
Junction-to-Ambient ³	R _{θJA}		50	

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

³50°C / W when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ($T_c = 25\text{ }^{\circ}\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1	-1.5	-3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -24V, V_{GS} = 0V$			-1	μA
		$V_{DS} = -20V, V_{GS} = 0V, T_J = 125\text{ }^{\circ}C$			-10	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = -5V, V_{GS} = -10V$	-50			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = -10V, I_D = -20A$		10.5	12	m Ω
		$V_{GS} = -4.5V, I_D = -10A$		15	20	
Forward Transconductance ¹	g_{fs}	$V_{DS} = -5V, I_D = -20A$		30		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -15V, f = 1MHz$		2363		pF
Output Capacitance	C_{oss}			385		
Reverse Transfer Capacitance	C_{rss}			326		
Gate Resistance	R_g	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		4.0		Ω
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = -15V, V_{GS} = -10V,$ $I_D = -20A$		45		nC
Gate-Source Charge ^{1,2}	Q_{gs}			5.6		
Gate-Drain Charge ^{1,2}	Q_{gd}			8.5		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = -15V,$ $I_D = -1A, V_{GS} = -10V, R_{GS} = 2.7\Omega$		15		nS
Rise Time ^{1,2}	t_r			12		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			35		
Fall Time ^{1,2}	t_f			10		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_c = 25\text{ }^{\circ}C$)						
Continuous Current	I_S				-50	A
Pulsed Current ³	I_{SM}				-120	
Forward Voltage ¹	V_{SD}	$I_F = -20A, V_{GS} = 0V$			-1.2	V
Reverse Recovery Time	t_{rr}	$I_F = I_S, dI_F/dt = 100A / \mu S$		32		nS
Reverse Recovery Charge	Q_{rr}			26		nC

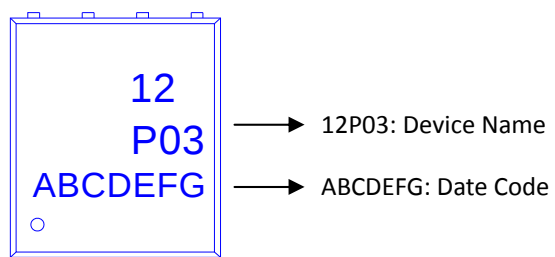
¹Pulse test : Pulse Width $\leq 300\text{ }\mu\text{sec}$, Duty Cycle $\leq 2\%$.

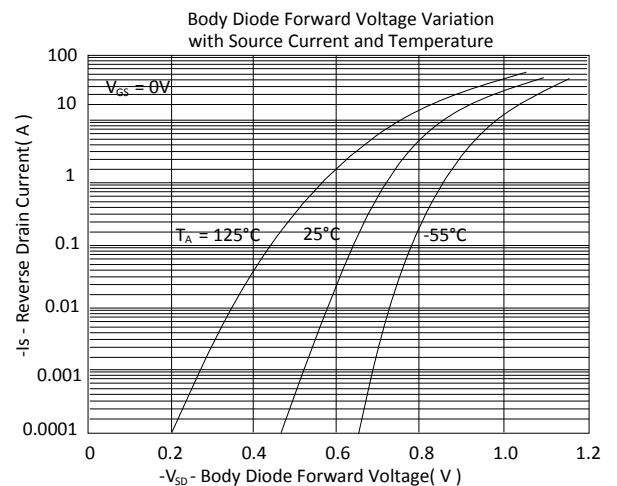
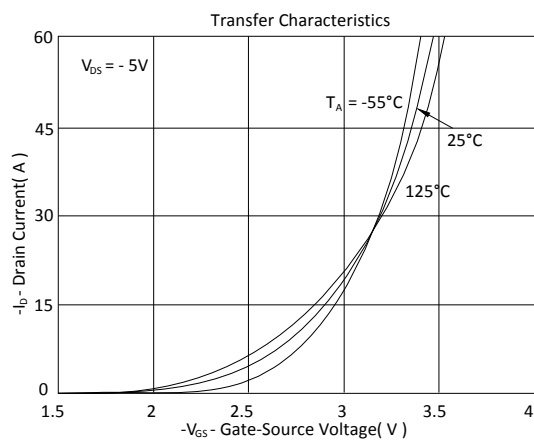
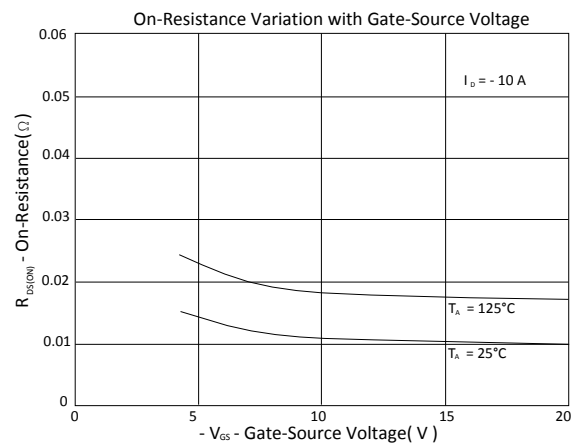
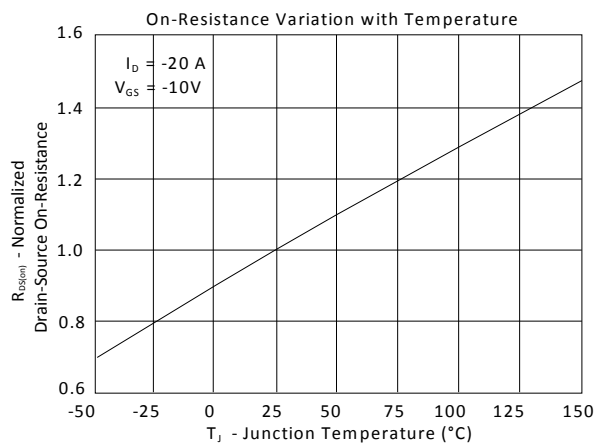
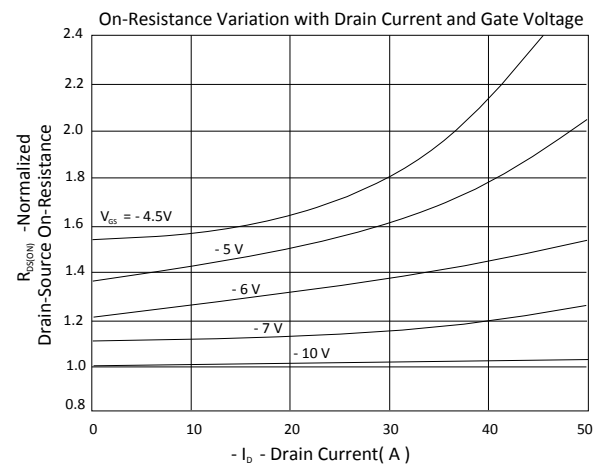
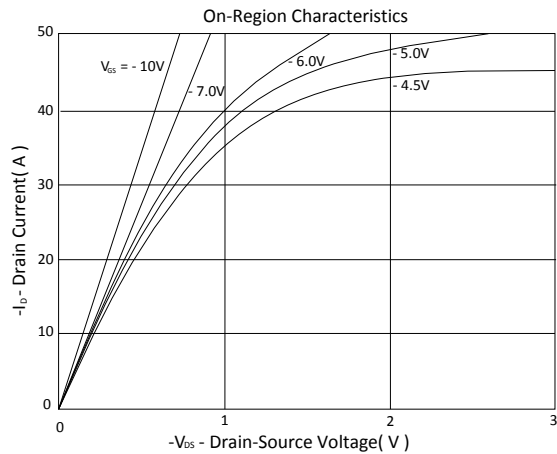
²Independent of operating temperature.

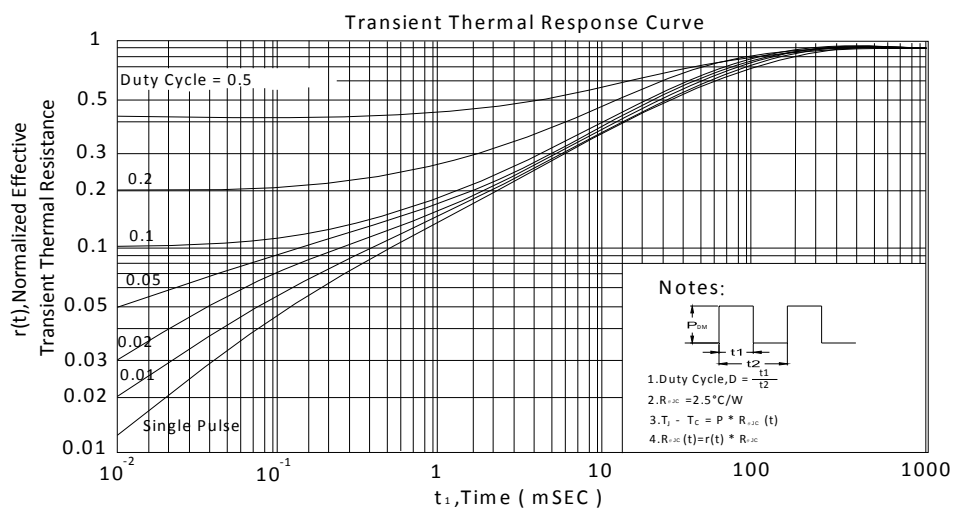
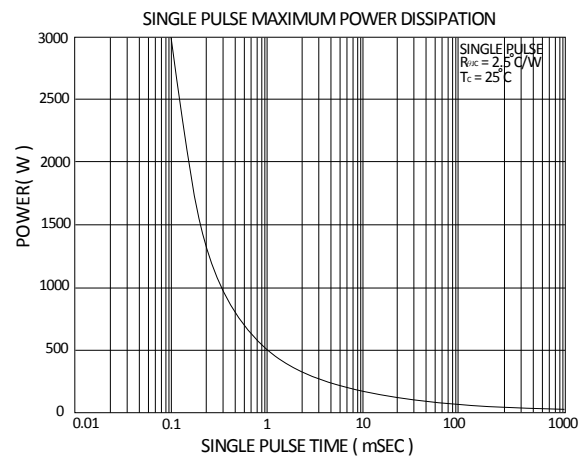
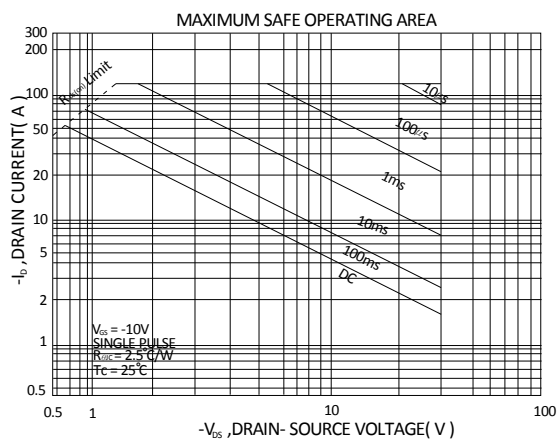
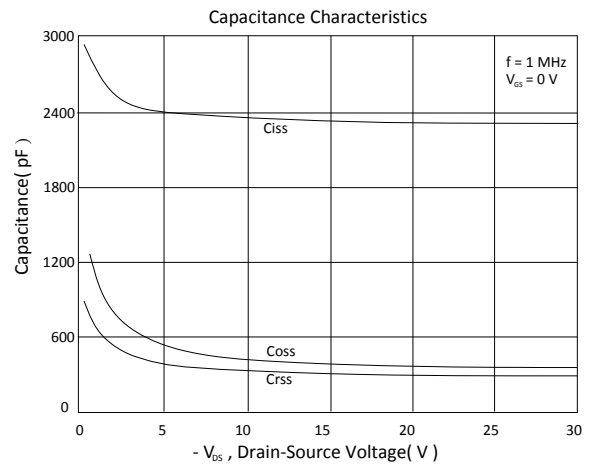
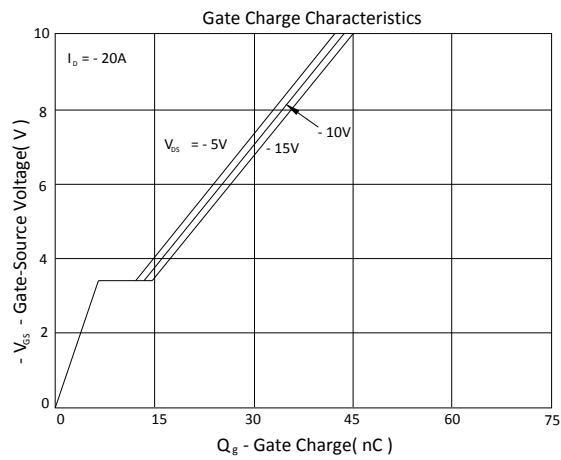
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

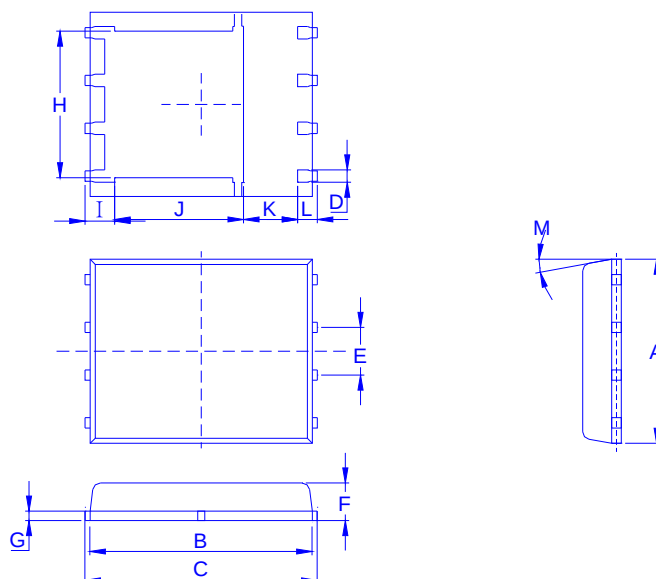
Device Name: LB12P03C for EDFN 5 x 6







Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K	L	M
Min.	4.80	5.50	5.90	0.3		0.85	0.15	3.67	0.41	3.00	0.94	0.45	0°
Typ.					1.27								
Max.	5.30	5.90	6.15	0.51		1.20	0.30	4.54	0.85	3.92	1.7	0.71	12°

Recommended minimum pads

