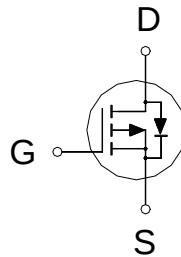


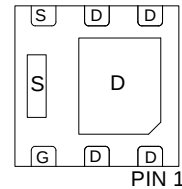
P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-20V
$R_{DS(on)} (MAX.)$	100m Ω
I_D	-3.4A



Bottom View



Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 12	V
Continuous Drain Current	$T_A = 25^\circ\text{C}$	I_D	-3.4	A
	$T_A = 70^\circ\text{C}$		-2.4	
Pulsed Drain Current ¹		I_{DM}	-13.6	
Power Dissipation	$T_A = 25^\circ\text{C}$	P_D	2.08	W
	$T_A = 70^\circ\text{C}$		1.33	
Operating Junction & Storage Temperature Range		$T_{j, T_{stg}}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		20	$^\circ\text{C} / \text{W}$
Junction-to-Ambient ³	$R_{\theta JA}$		60	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³60 $^\circ\text{C} / \text{W}$ when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-20			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-0.3	-0.75	-1.2	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -16V, V _{GS} = 0V			-1	μA
		V _{DS} = -16V, V _{GS} = 0V, T _J = 125 °C			-10	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = -5V, V _{GS} = -4.5V	-3.4			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = -4.5V, I _D = -3.4A		83	100	mΩ
		V _{GS} = -2.5V, I _D = -2.5A		110	135	
Forward Transconductance ¹	g _{fs}	V _{DS} = -5V, I _D = -3A		4.5		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = -10V, f = 1MHz		450		pF
Output Capacitance	C _{oss}			58		
Reverse Transfer Capacitance	C _{rss}			41		
Total Gate Charge ^{1,2}	Q _g	V _{DS} = -10V, V _{GS} = -4.5V, I _D = -3A		5.4		nC
Gate-Source Charge ^{1,2}	Q _{gs}			1.0		
Gate-Drain Charge ^{1,2}	Q _{gd}			1.3		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{DS} = -10V, I _D = -1A, V _{GS} = -4.5V, R _{GS} = 6Ω		10		nS
Rise Time ^{1,2}	t _r			20		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			15		
Fall Time ^{1,2}	t _f			12		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _C = 25 °C)						
Continuous Current	I _S				-3.4	A
Pulsed Current ³	I _{SM}				-13.6	
Forward Voltage ¹	V _{SD}	I _F = I _S , V _{GS} = 0V			-1.2	V

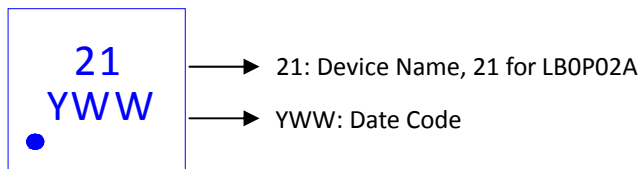
¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

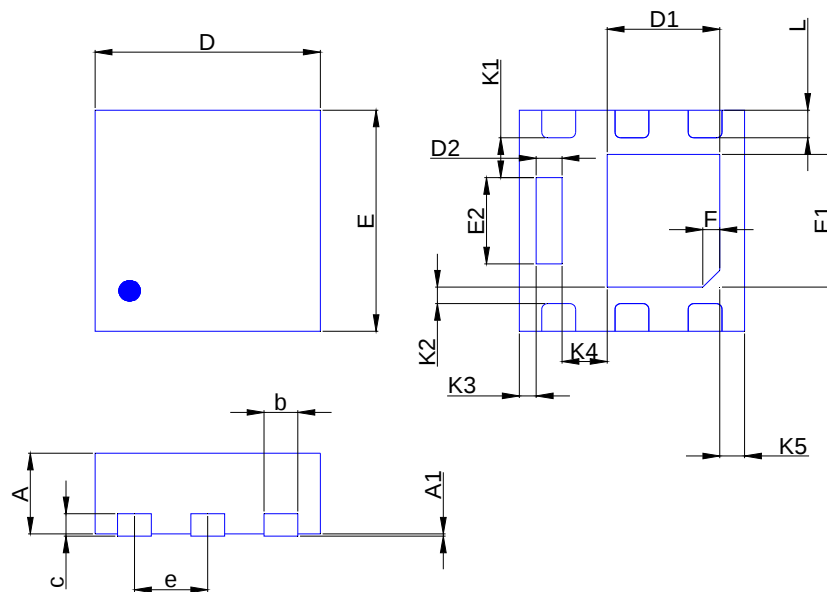
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: LB0P02A for EDFN 2 x 2



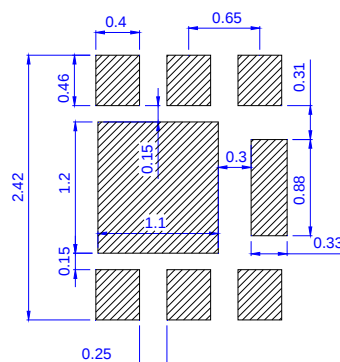
Outline Drawing



Dimension in mm

Dimension	A	A1	b	c	D	D1	D2	E	E1	E2	e	F	f	K1	K2	L	K3	K4	K5
Min.	0.50	0.00	0.25		1.9	1.0	0.13	1.9	1.1	0.65				0.306	0.10	0.2	0.10	0.27	0.17
Typ.		0.02	0.30	0.1	2.0	1.1	0.25	2.0	1.2	0.75	0.65	0.15	45°	0.356	0.15	0.25	0.15		0.22
Max.	0.65	0.05	0.35		2.1	1.2	0.35	2.1	1.3	0.88				0.406	0.20	0.3	0.20		0.27

Recommended minimum pads



TYPICAL CHARACTERISTICS

