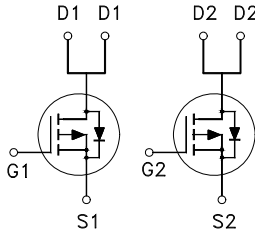
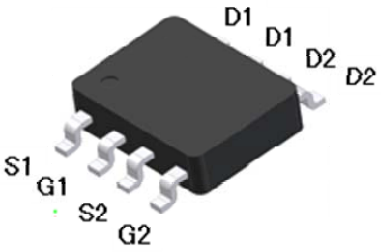
Dual P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-20V
$R_{DSON\ (MAX.)}$	100mΩ
I_D	-3A





Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current	T_A = 25 °C	I_D	-3	A
	T_A = 70 °C		-2.4	
Pulsed Drain Current[1]		I_{DM}	-16	
Power Dissipation	T_A = 25 °C	P_D	2	W
	T_A = 70 °C		1.2	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		25	°C / W
Junction-to-Ambient[3]	$R_{\theta JA}$		62.5	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

[3]62.5°C / W when mounted on a 1 in^2 pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_A = 25 °C, Unless Otherwise Noted)

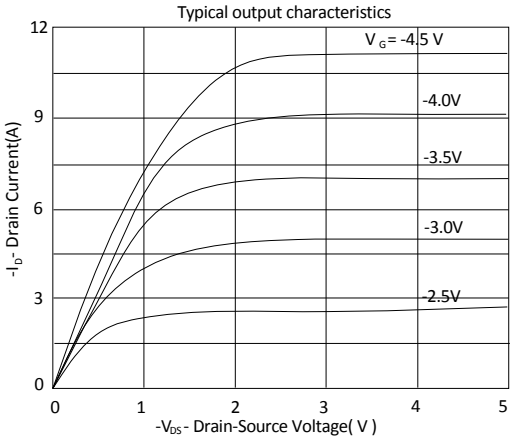
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-0.3	-0.75	-1.2	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -16V, V_{GS} = 0V			-1	μA
		V_{DS} = -16V, V_{GS} = 0V, T_J = 125 °C			-10	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -4.5V	-3			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -4.5V, I_D = -3A		85	100	mΩ
		V_{GS} = -2.5V, I_D = -2.5A		120	150	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -3A		4.5		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -10V, f = 1MHz		382		pF
Output Capacitance	C_{oss}			70		
Reverse Transfer Capacitance	C_{rss}			60		
Total Gate Charge[1,2]	Q_g	V_{DS} = -10V, V_{GS} = -4.5V, I_D = -3A		7.2		nC
Gate-Source Charge[1,2]	Q_{gs}			1.2		
Gate-Drain Charge[1,2]	Q_{gd}			2.3		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = -10V, I_D = -1A, V_{GS} = -4.5V, R_{GS} = 6Ω		10		nS
Rise Time[1,2]	t_r			20		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			15		
Fall Time[1,2]	t_f			12		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				-2.3	A
Pulsed Current[3]	I_{SM}				-9.2	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			1.2	V

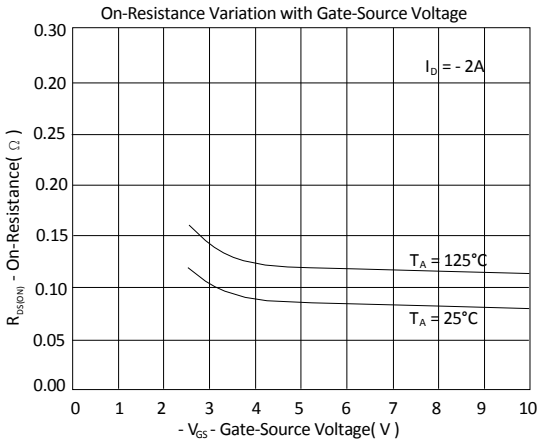
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

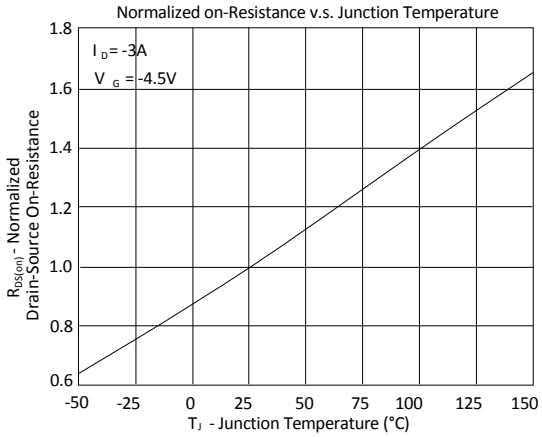
[2]Independent of operating temperature.

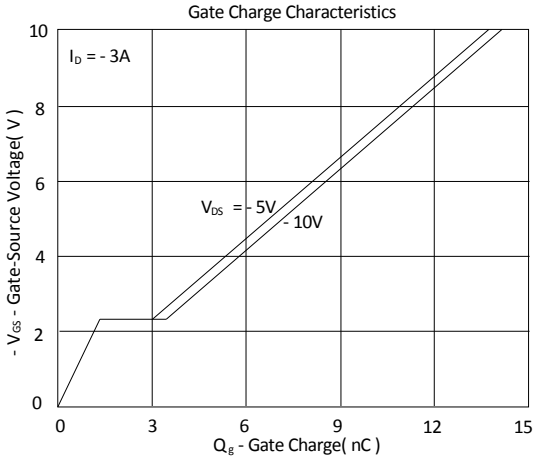
[3]Pulse width limited by maximum junction temperature.

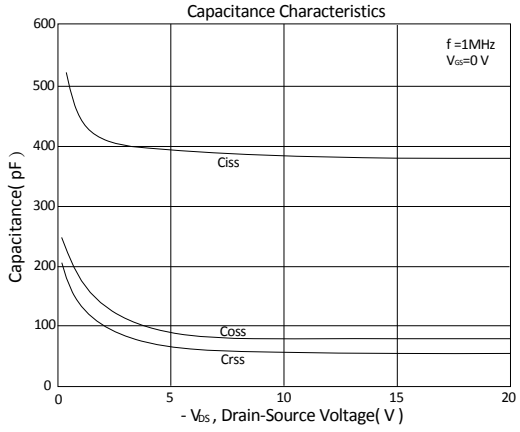
TYPICAL CHARACTERISTICS

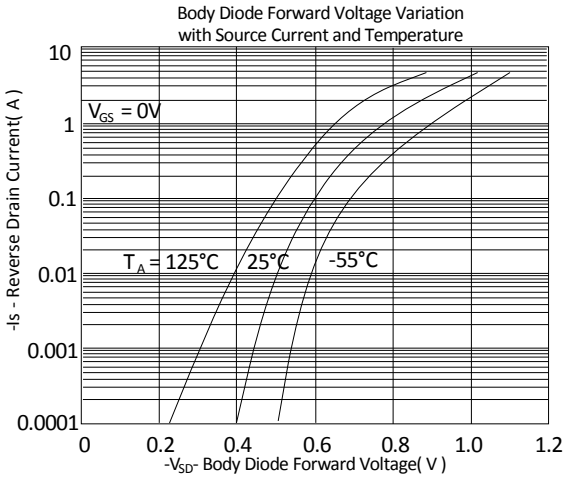


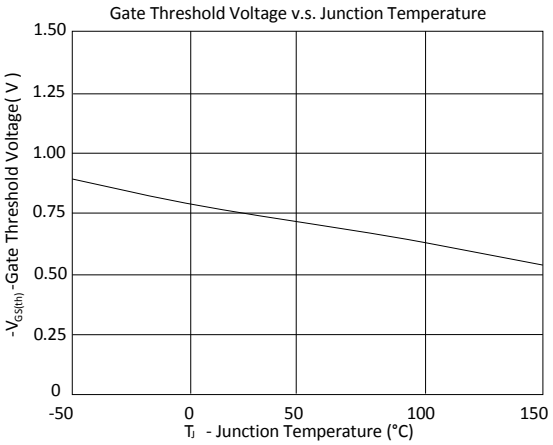


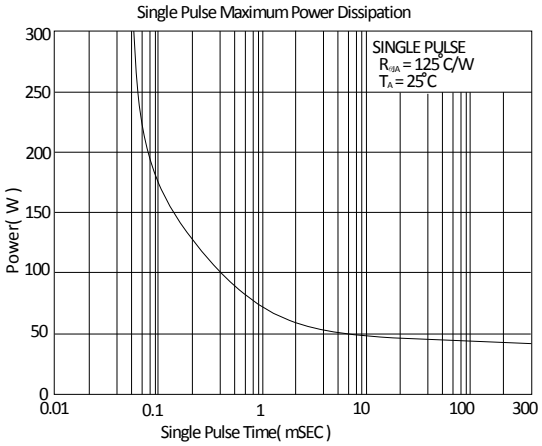


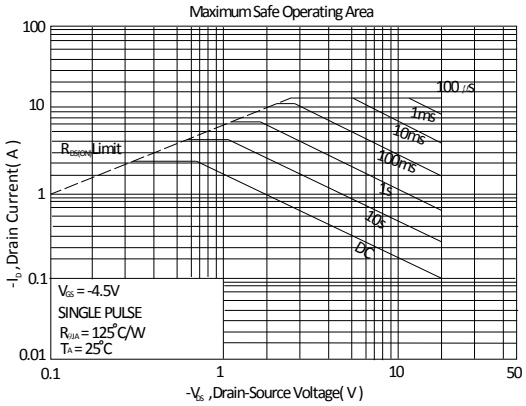


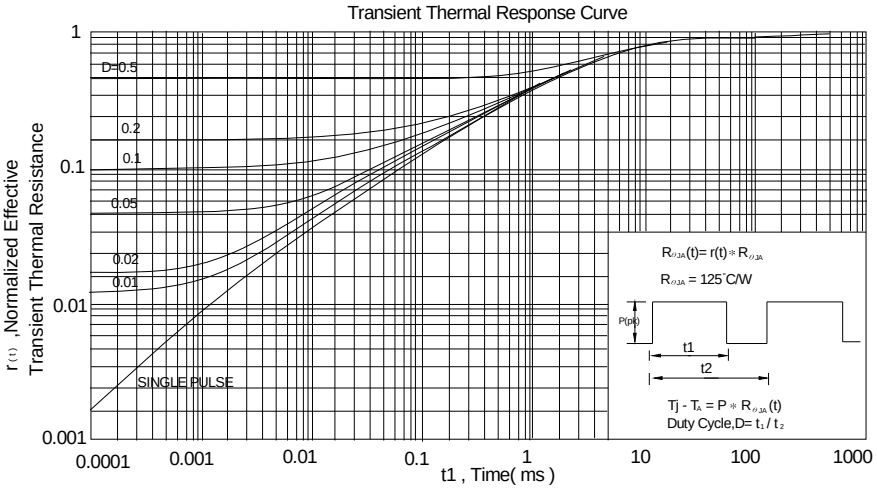





Gate Threshold Voltage v.s. Junction Temperature
-VGS(th) -Gate Threshold Voltage(V)
1.50
1.25
1.00
0.75
0.50
0.25
0
-50
0
50
100
150
Tj - Junction Temperature (°C)

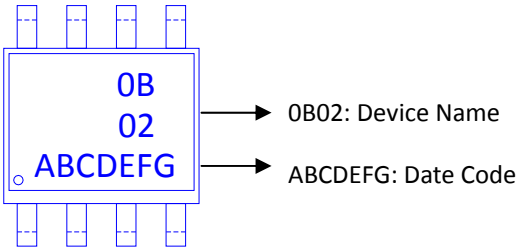

Single Pulse Maximum Power Dissipation
SINGLE PULSE
RθJA = 125°C/W
TA = 25°C
Power(W)
300
250
200
150
100
50
0
0.01
0.1
1
10
100
300
Single Pulse Time(mSEC)


Maximum Safe Operating Area
-ID, Drain Current(A)
100
10
1
0.1
0.01
RDS(ON) Limit
100μs
1ms
10ms
100ms
1s
10s
DC
VGS = -4.5V
SINGLE PULSE
RθJA = 125°C/W
TA = 25°C
0.1
1
10
50
-VDS ,Drain-Source Voltage(V)

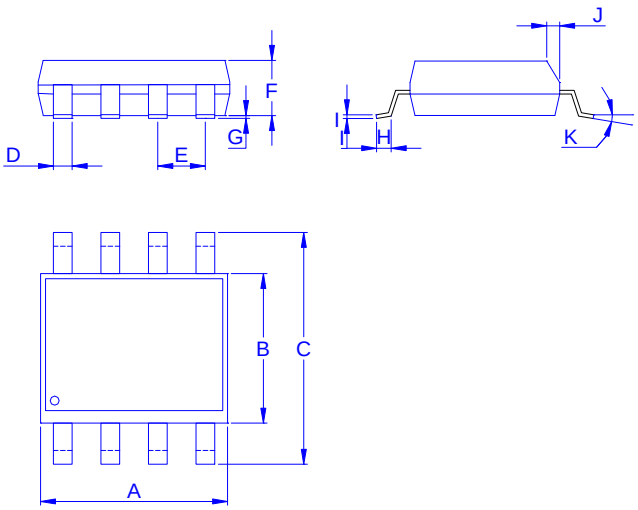

Transient Thermal Response Curve
r(t) ,Normalized Effective Transient Thermal Resistance
1
0.1
0.01
0.001
D=0.5
0.2
0.1
0.05
0.02
0.01
SINGLE PULSE
RθJA(t)= r(t)＊RθJA
RθJA = 125°C/W
P(pk)
t1
t2
Tj - TA = P＊RθJA(t)
Duty Cycle,D= t1 / t2
0.0001
0.001
0.01
0.1
1
10
100
1000
t1 , Time(ms)

Ordering & Marking Information:

Device Name: LB0B02HD for SOP-8



Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°