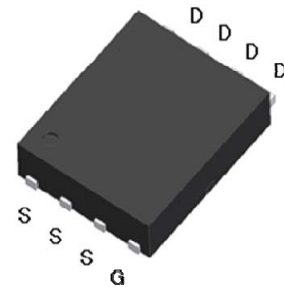
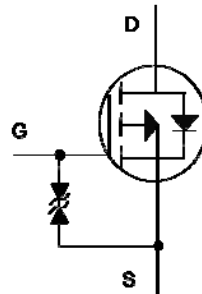


P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-30V
$R_{DS(on)} (MAX.)$	8.5m Ω
I_D	-70A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

ESD Protection



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25^\circ\text{C}$	I_D	-70	A
	$T_C = 100^\circ\text{C}$		-50	
Pulsed Drain Current ¹		I_{DM}	-150	
Avalanche Current		I_{AS}	-50	
Avalanche Energy	$L = 0.1\text{mH}, I_D = -50\text{A}, R_G = 25\Omega$	E_{AS}	125	mJ
Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	50	W
	$T_C = 100^\circ\text{C}$		20	
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150	$^\circ\text{C}$

100% UIS testing in condition of $V_D = -15\text{V}$, $L = 0.1\text{mH}$, $V_G = -10\text{V}$, $I_L = -40\text{A}$, Rated $V_{DS} = -30\text{V}$ P-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		2.5	$^\circ\text{C} / \text{W}$
Junction-to-Ambient ³	$R_{\theta JA}$		50	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-1	-1.5	-3	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±12V			±10	μA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -24V, V _{GS} = 0V			-1	μA
		V _{DS} = -20V, V _{GS} = 0V, T _J = 125 °C			-10	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = -5V, V _{GS} = -10V	-70			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = -10V, I _D = -15A		7	8.5	mΩ
		V _{GS} = -4.5V, I _D = -12A		12	15	
Forward Transconductance ¹	g _{fs}	V _{DS} = -5V, I _D = -15A		26		S
DYNAMIC						
Input Capacitance	C _{iSS}	V _{GS} = 0V, V _{DS} = -15V, f = 1MHz		3091		pF
Output Capacitance	C _{oSS}			476		
Reverse Transfer Capacitance	C _{rSS}			404		
Gate Resistance	R _g	V _{GS} = 15mV, V _{DS} = 0V, f = 1MHz		3.5		Ω
Total Gate Charge ^{1,2}	Q _g (V _{GS} =10V)	V _{DS} = -15V, V _{GS} = -10V, I _D = -15A		54		nC
	Q _g (V _{GS} =4.5V)			32		
Gate-Source Charge ^{1,2}	Q _{gs}			7.3		
Gate-Drain Charge ^{1,2}	Q _{gd}			13		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{DS} = -15V, I _D = -1A, V _{GS} = -10V, R _{GS} = 2.7Ω		24		nS
Rise Time ^{1,2}	t _r			20		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			70		
Fall Time ^{1,2}	t _f			12		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _C = 25 °C)						
Continuous Current	I _S				-70	A
Pulsed Current ³	I _{SM}				-150	
Forward Voltage ¹	V _{SD}	I _F = -15A, V _{GS} = 0V			-1.2	V
Reverse Recovery Time	t _{rr}	I _F = I _S , dI _F /dt = 100A / μS		52		nS
Reverse Recovery Charge	Q _{rr}			60		nC

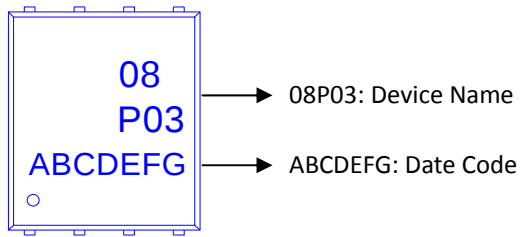
¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

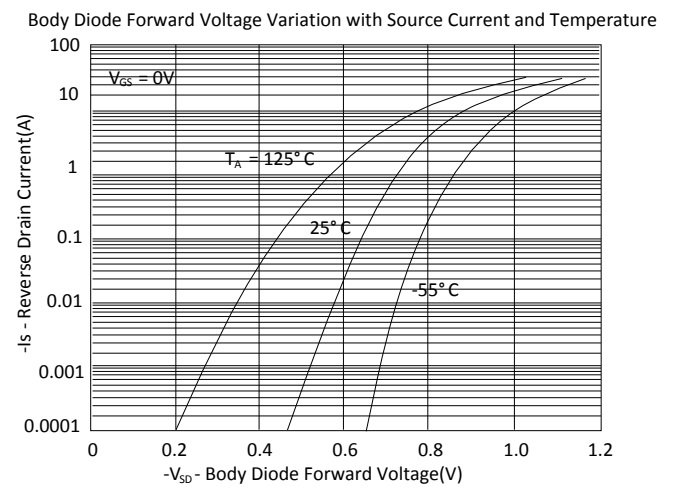
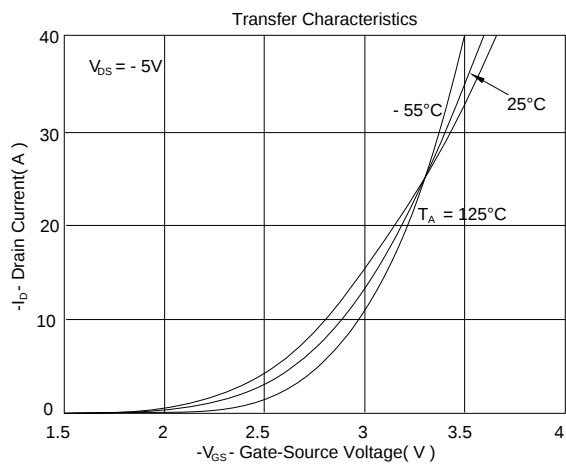
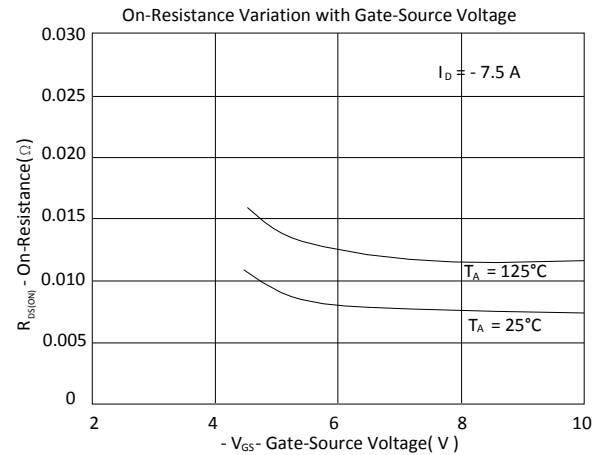
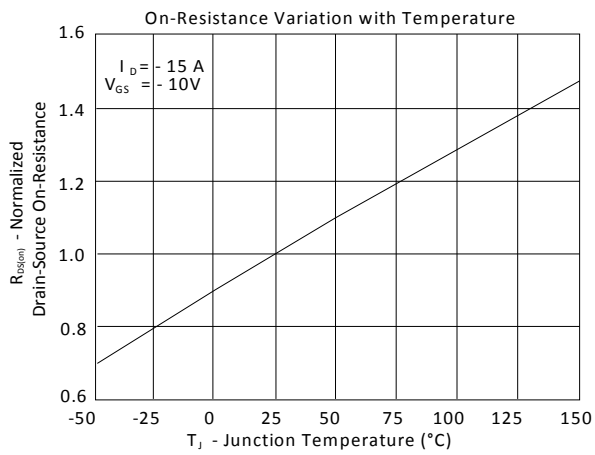
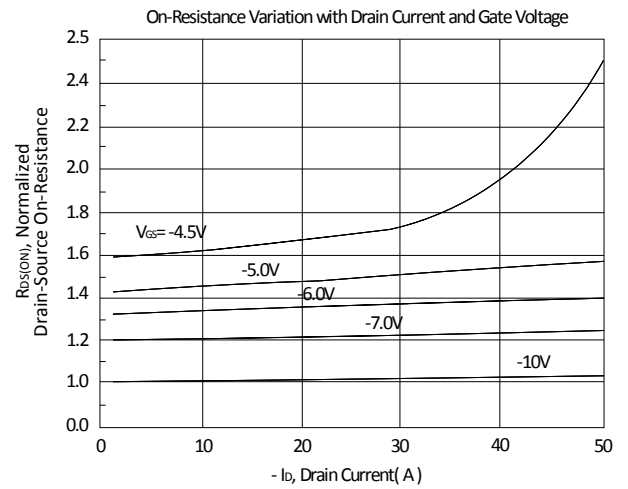
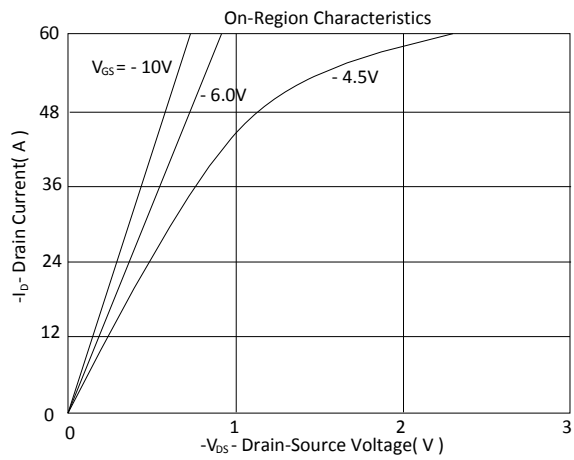
²Independent of operating temperature.

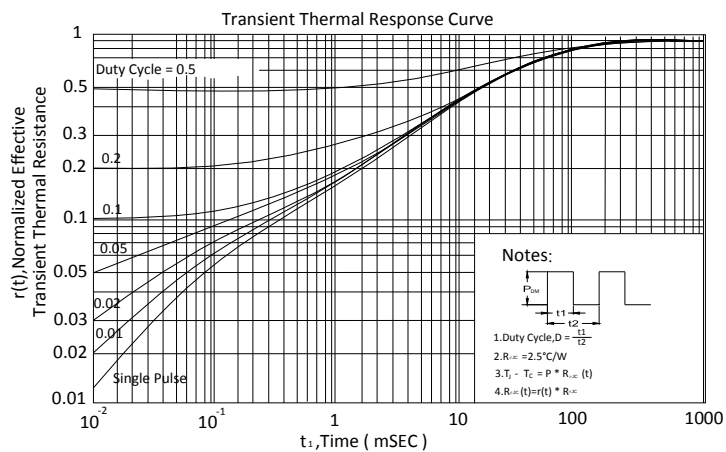
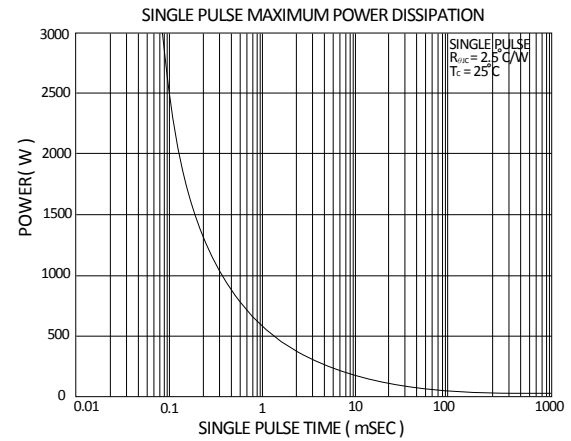
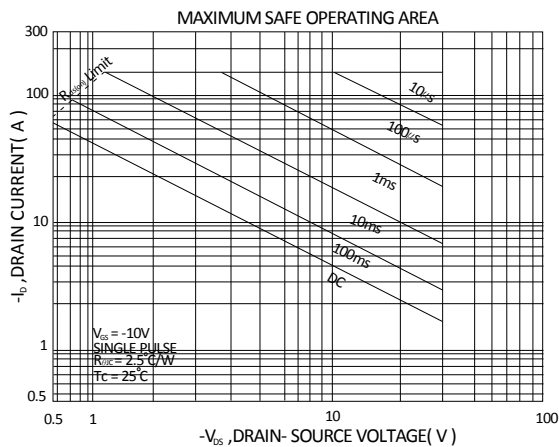
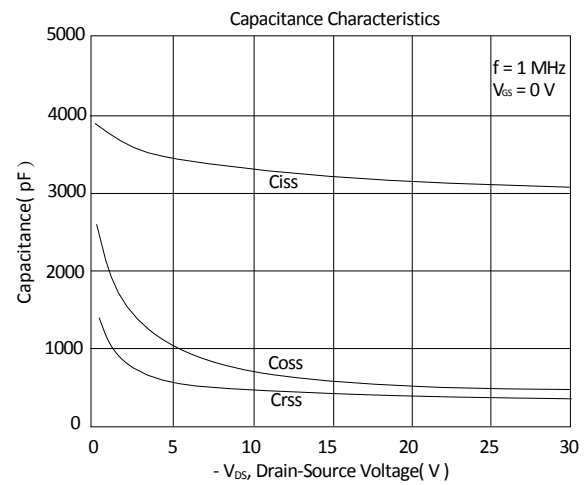
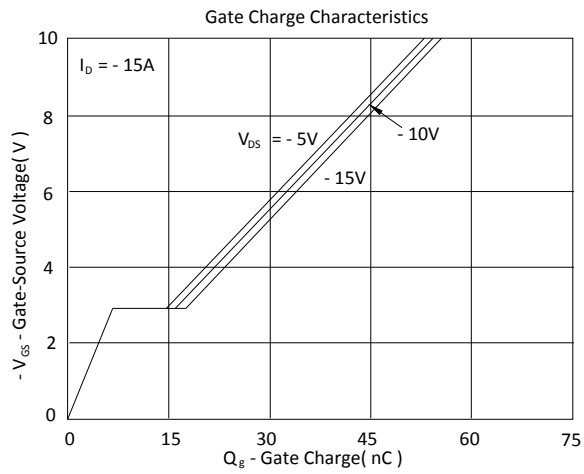
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

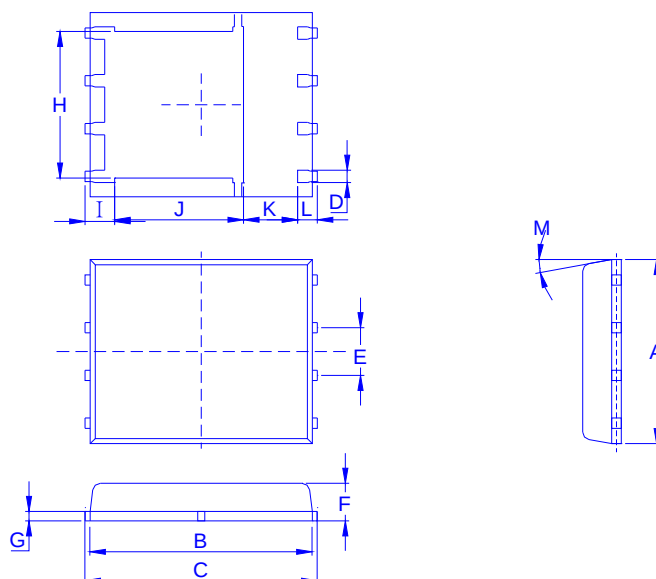
Device Name: LB08P03C for EDFN 5 x 6







Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K	L	M
Min.	4.80	5.50	5.90	0.3		0.85	0.15	3.67	0.41	3.00	0.94	0.45	0°
Typ.					1.27								
Max.	5.30	5.90	6.15	0.51		1.20	0.30	4.54	0.85	3.92	1.7	0.71	12°

Recommended minimum pads

