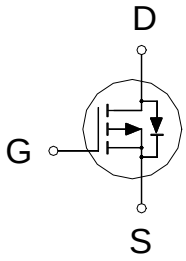
P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-20V
$R_{DSON\ (MAX.)}$	3.2mΩ
I_D	-100A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current[1]	T_C = 25 °C	I_D	-100	A
	T_C = 100 °C		-73	
Pulsed Drain Current[2]		I_{DM}	-400	
Avalanche Current		I_{AS}	-100	
Avalanche Energy	L = 0.1mH, ID=-100A, RG=25Ω	E_{AS}	500	mJ
Repetitive Avalanche Energy[3]	L = 0.05mH	E_{AR}	250	
Power Dissipation	T_C = 25 °C	P_D	69	W
	T_C = 100 °C		27	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

100% UIS testing in condition of V_D=-15V, L=0.1mH, V_G=-5V, I_L=-70A, Rated V_{DS}=-20V P-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		1.8	°C / W
Junction-to-Ambient[4]	$R_{\theta JA}$		50	

[1]Package Limited.

[2]Pulse width limited by maximum junction temperature.

[3]Duty cycle ≤ 1%

[4]50°C / W when mounted on a 1 in^2 pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-0.4	-0.6	-1.2	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -16V, V_{GS} = 0V			-1	μA
		V_{DS} = -12V, V_{GS} = 0V, T_J = 125 °C			-10	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -4.5V	-100			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -10V, I_D = -20A		2.4	2.7	mΩ
		V_{GS} = -4.5V, I_D = -20A		2.7	3.2	
		V_{GS} = -2.5V, I_D = -20A		3.4	4.1	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -20A		65		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -10V, f = 1MHz		11116		pF
Output Capacitance	C_{oss}			1303		
Reverse Transfer Capacitance	C_{rss}			592		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz		3		Ω
Total Gate Charge[1,2]	Q_g(V_{GS}=-10V)	V_{DS} = -10V, V_{GS} = -10V, I_D = -20A		202		nC
	Q_g(V_{GS}=-4.5V)			87		
Gate-Source Charge[1,2]	Q_{gs}			18		
Gate-Drain Charge[1,2]	Q_{gd}			16		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = -10V, I_D = -1A, V_{GS} = -10V, R_{GS} = 3Ω		20		nS
Rise Time[1,2]	t_r			55		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			270		
Fall Time[1,2]	t_f			100		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				-100	A
Pulsed Current[3]	I_{SM}				-400	
Forward Voltage[1]	V_{SD}	I_F = -20A, V_{GS} = 0V			-1.2	V
Reverse Recovery Time	t_{rr}	I_F = -20A, dI_F/dt = 100A / μS		50		nS
Reverse Recovery Charge	Q_{rr}			180		nC

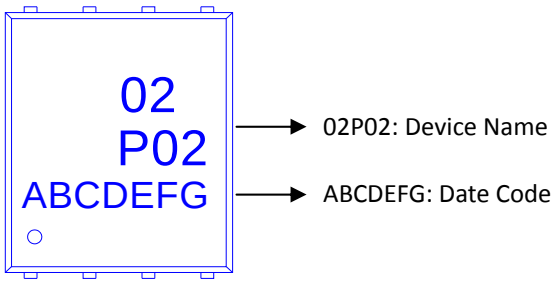
[1]Pulse test : Pulse Width ≤300μ sec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

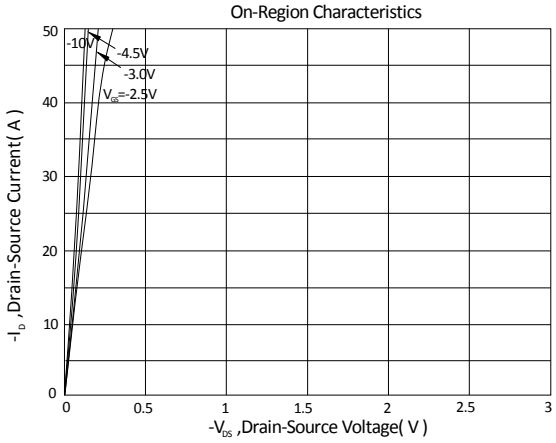
[3]Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

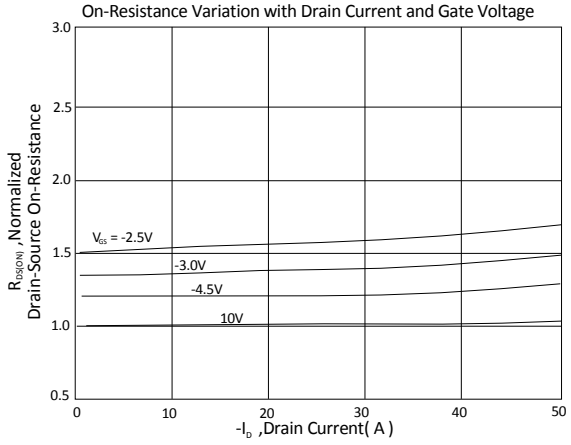
Device Name: LB02P02C for EDFN 5 x 6



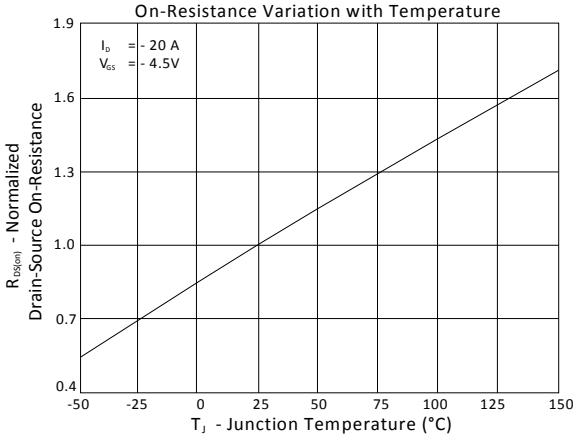
On-Region Characteristics



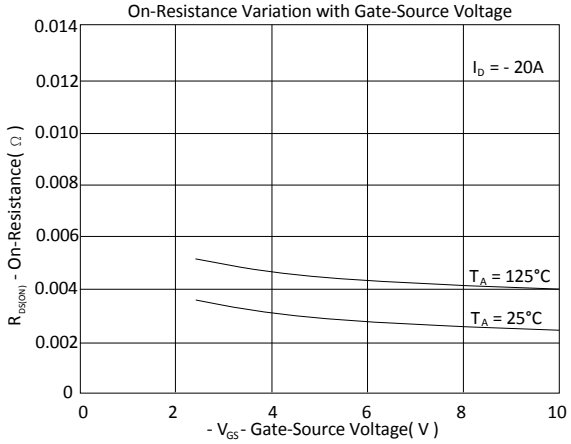
On-Resistance Variation with Drain Current and Gate Voltage



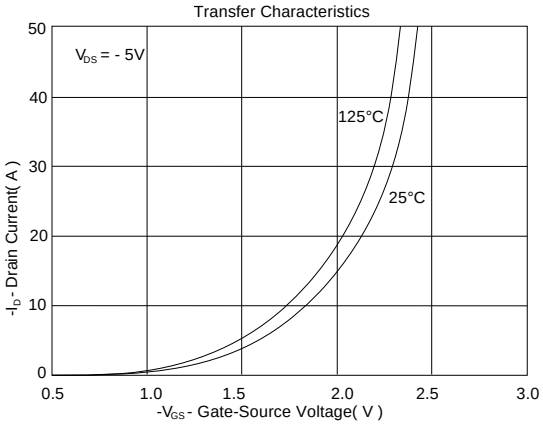
On-Resistance Variation with Temperature



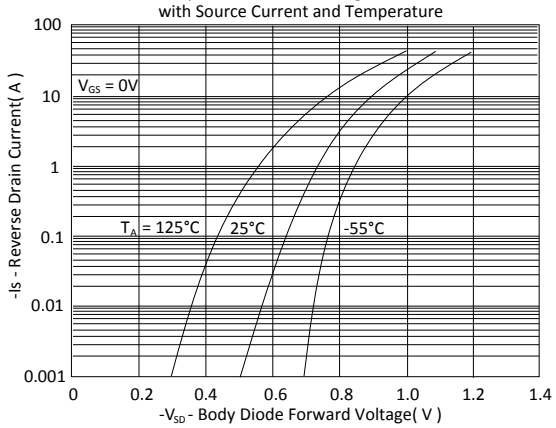
On-Resistance Variation with Gate-Source Voltage



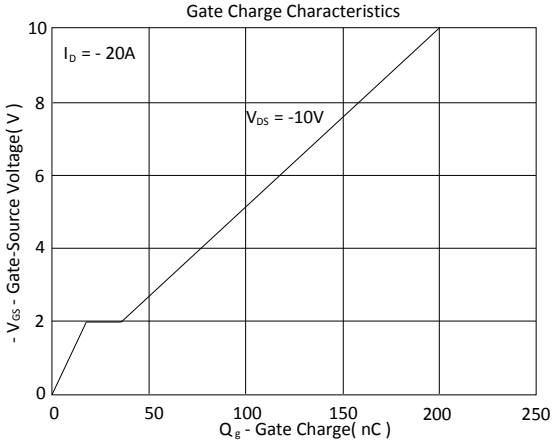
Transfer Characteristics



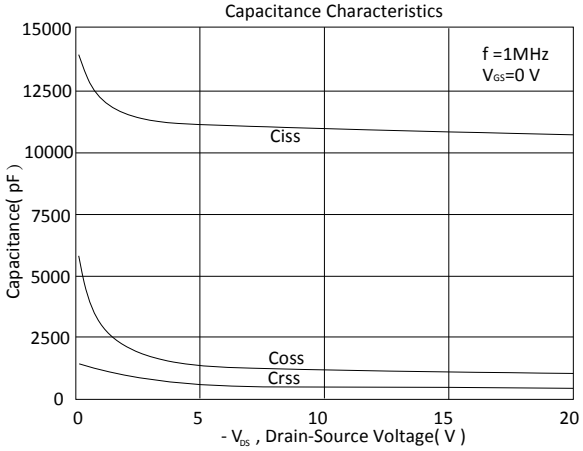
Body Diode Forward Voltage Variation
with Source Current and Temperature



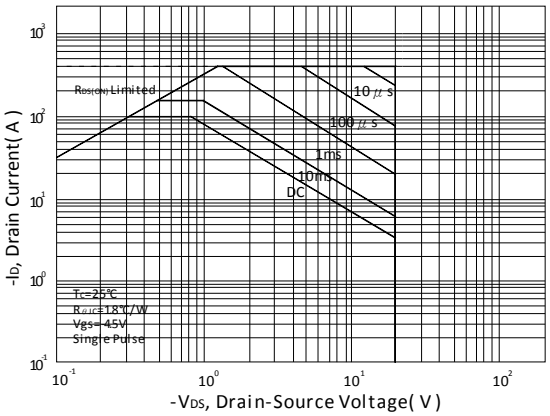
Gate Charge Characteristics



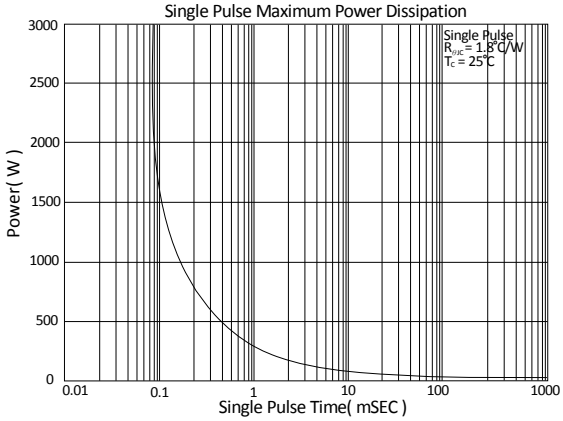
Capacitance Characteristics



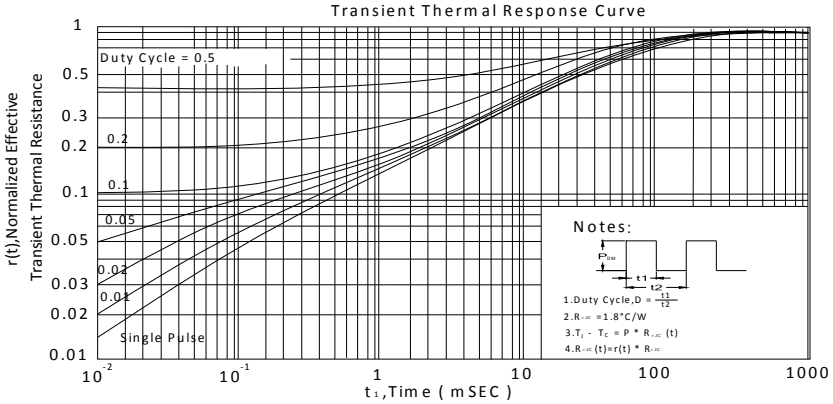
Maximum Safe Operating Area



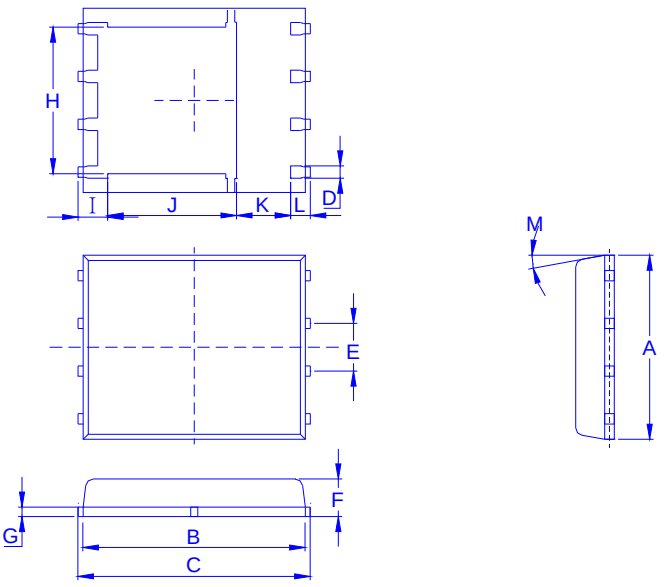
Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K	L	M
Min.	4.80	5.50	5.90	0.3		0.85	0.15	3.67	0.41	3.00	0.94	0.45	0°
Typ.					1.27								
Max.	5.30	5.90	6.15	0.51		1.20	0.30	4.54	0.85	3.92	1.7	0.71	12°

Recommended minimum pads