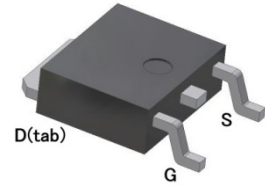
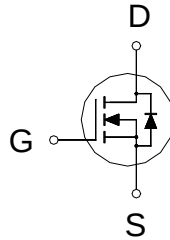


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	600V
$R_{DS(on)} (MAX.)$	1.55Ω
I_D	6A



UIS, 100% Tested

Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 30	V
Continuous Drain Current	$T_C = 25^\circ\text{C}$	I_D	6	A
	$T_C = 100^\circ\text{C}$		3.7	
Pulsed Drain Current ¹		I_{DM}	24	
Avalanche Current		I_{AS}	6	mJ
Avalanche Energy	$L = 3\text{mH}, I_D = 6\text{A}, R_G = 25 \Omega$	E_{AS}	54	
Repetitive Avalanche Energy ²	$L = 0.5\text{mH}$	E_{AR}	9	
Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	48	W
	$T_C = 100^\circ\text{C}$		19	
Operating Junction & Storage Temperature Range		$T_{j, T_{stg}}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		2.6	$^\circ\text{C} / \text{W}$
Junction-to-Ambient	$R_{\theta JA}$		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

ELECTRICAL CHARACTERISTICS (T_c = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	600			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	2	3	4	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±30V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 600V, V _{GS} = 0V			10	μA
		V _{DS} = 480V, V _{GS} = 0V, T _J = 125 °C			25	
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 10V, I _D = 3A		1.4	1.55	Ω
Forward Transconductance ¹	g _{fs}	V _{DS} = 25V, I _D = 3A		6		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 25V, f = 1MHz		660		pF
Output Capacitance	C _{oss}			70		
Reverse Transfer Capacitance	C _{rss}			3.5		
Total Gate Charge ^{1,2}	Q _g	V _{DS} = 300V, V _{GS} = 15V, I _D = 3A		11.5		nC
Gate-Source Charge ^{1,2}	Q _{gs}			2.9		
Gate-Drain Charge ^{1,2}	Q _{gd}			3.1		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{DS} = 300V, I _D = 3A, V _{GS} = 15V, R _{GS} = 10Ω		12		nS
Rise Time ^{1,2}	t _r			10		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			26		
Fall Time ^{1,2}	t _f			10		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _c = 25 °C)						
Continuous Current	I _S				6	A
Pulsed Current ³	I _{SM}				24	
Forward Voltage ¹	V _{SD}	I _F = I _S , V _{GS} = 0V			1.5	V
Reverse Recovery Time	t _{rr}	I _F = I _S , dI _F /dt = 100A / μS		0.8		μS
Reverse Recovery Charge	Q _{rr}			3.6		nC

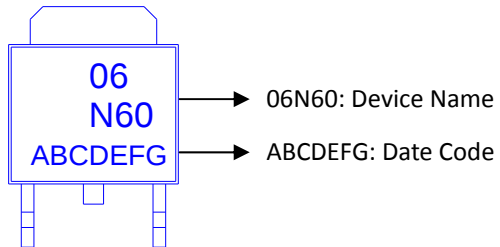
¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

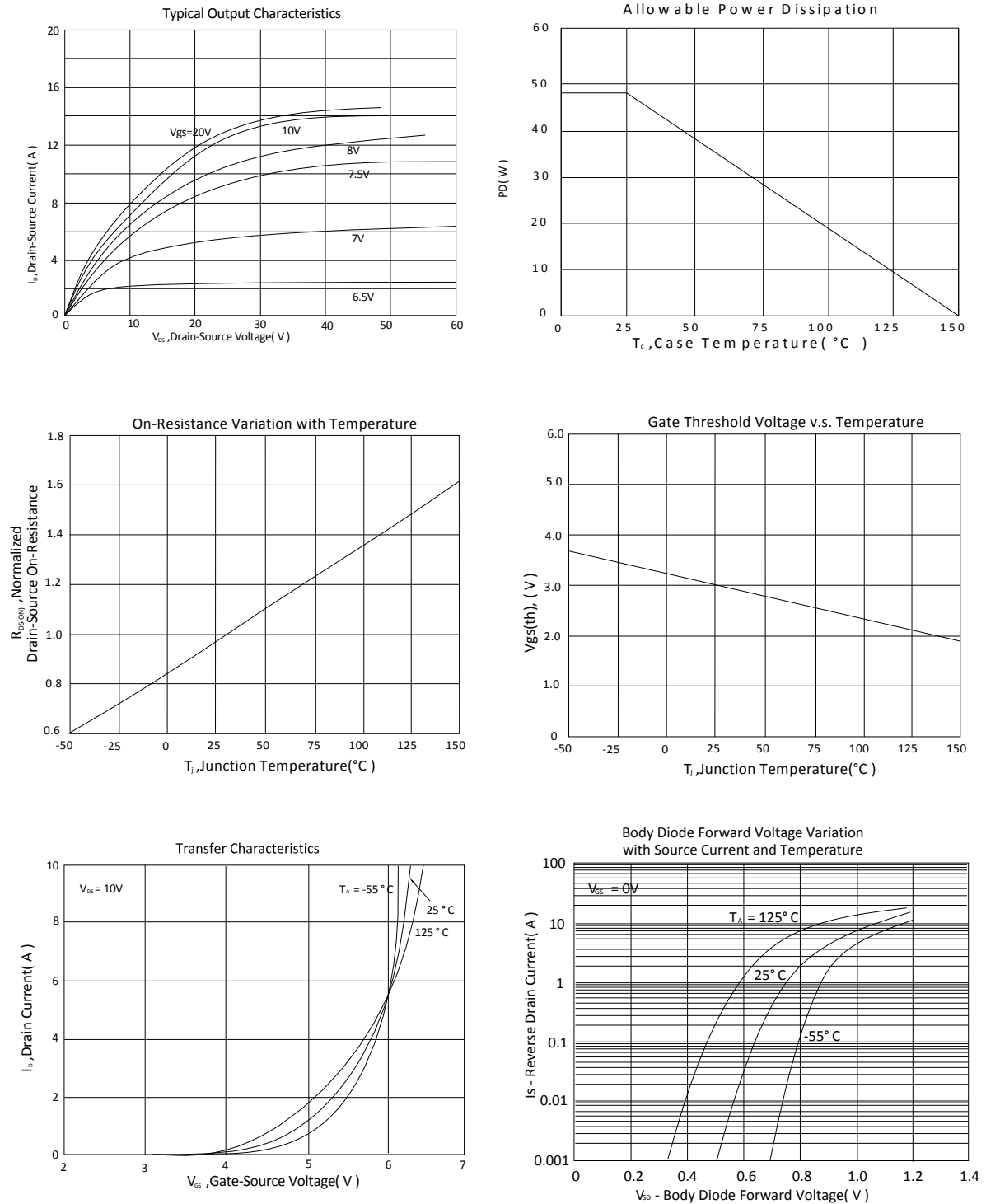
³Pulse width limited by maximum junction temperature.

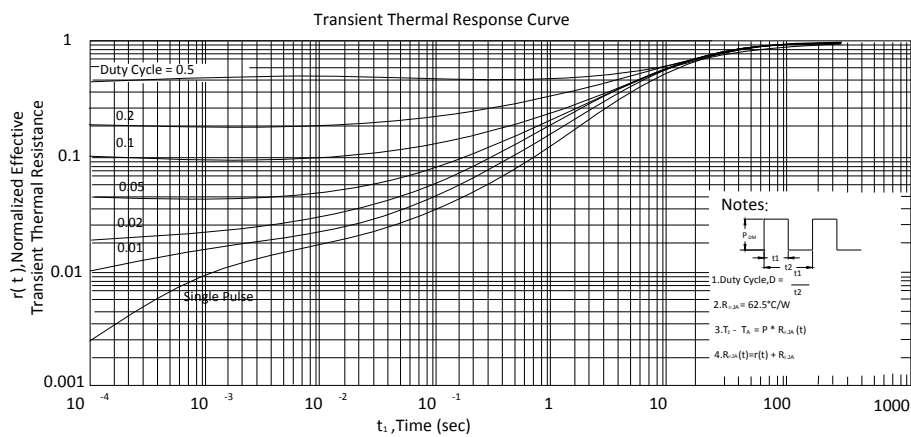
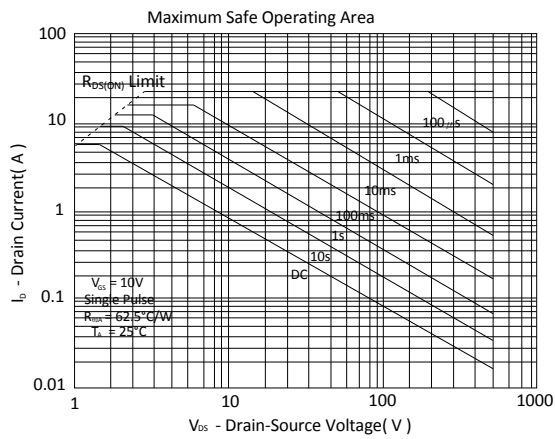
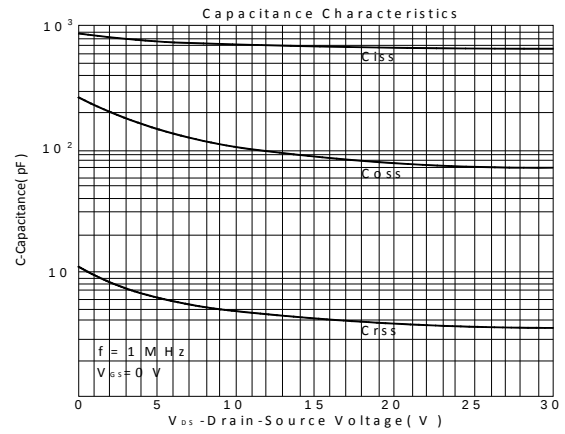
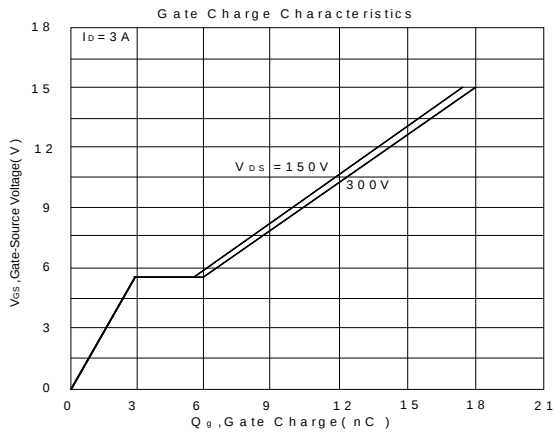
Ordering & Marking Information:

Device Name: LB06N60D for DPAK (TO-252)

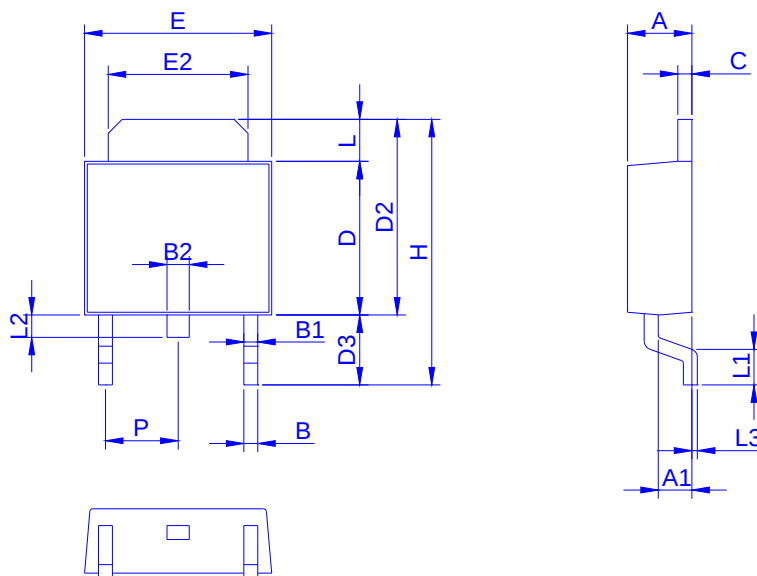


TYPICAL CHARACTERISTICS





Outline Drawing



Dimension in mm

Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	0.95	0.30	0.40	0.60	0.40	5.30	6.70	2.20	6.40	4.80	9.20	0.89	0.90	0.50	0.00	2.10
Max.	2.50	1.30	0.85	0.94	1.00	0.60	6.20	7.30	3.00	6.70	5.45	10.15	1.70	1.65	1.10	0.30	2.50

Footprint

