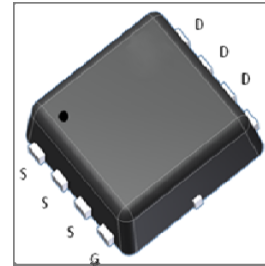


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	30V
R _{DS(on)} (MAX.)	6mΩ
I _D	26A



UIS, R_g 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _C = 25 °C	I _D	26	A
	T _C = 100 °C		18.5	
Pulsed Drain Current ¹		I _{DM}	104	
Avalanche Current		I _{AS}	14	
Avalanche Energy	L = 0.1mH, I _D =14A, R _G =25Ω	E _{AS}	9.8	mJ
Repetitive Avalanche Energy ²	L = 0.05mH	E _{AR}	4.9	
Power Dissipation	T _C = 25 °C	P _D	25	W
	T _C = 100 °C		8	
Power Dissipation	T _A = 25 °C	P _D	2.5	W
	T _A = 100 °C		1	
Operating Junction & Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}		6	°C / W
Junction-to-Ambient ³	R _{θJA}		50	

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

³50°C / W when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ($T_c = 25\text{ }^{\circ}\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	1.5	3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24V, V_{GS} = 0V$			1	μA
		$V_{DS} = 20V, V_{GS} = 0V, T_J = 125\text{ }^{\circ}C$			25	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 10V, V_{GS} = 10V$	26			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 14A$		5	6	m Ω
		$V_{GS} = 4.5V, I_D = 10A$		7.5	9.5	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 14A$		25		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 15V, f = 1MHz$		1983		pF
Output Capacitance	C_{oss}			328		
Reverse Transfer Capacitance	C_{rss}			287		
Gate Resistance	R_g	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		1.2		Ω
Total Gate Charge ^{1,2}	$Q_g(V_{GS}=10V)$	$V_{DS} = 15V, V_{GS} = 10V,$ $I_D = 14A$		34.6		nC
	$Q_g(V_{GS}=4.5V)$			21		
Gate-Source Charge ^{1,2}	Q_{gs}			4.8		
Gate-Drain Charge ^{1,2}	Q_{gd}			9.7		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = 15V,$ $I_D = 1A, V_{GS} = 10V, R_{GS} = 6\Omega$		9		nS
Rise Time ^{1,2}	t_r			20		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			25		
Fall Time ^{1,2}	t_f			3		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_c = 25\text{ }^{\circ}C$)						
Continuous Current	I_S				4	A
Pulsed Current ³	I_{SM}				16	
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			1.2	V
Reverse Recovery Time	t_{rr}	$I_F = I_S, dI_F/dt = 100A / \mu S$		32		nS
Peak Reverse Recovery Current	$I_{RM(REC)}$			40		A
Reverse Recovery Charge	Q_{rr}			12		nC

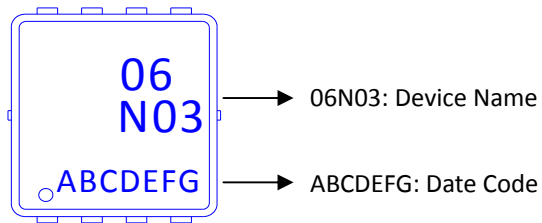
¹Pulse test : Pulse Width $\leq 300\mu$ sec, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

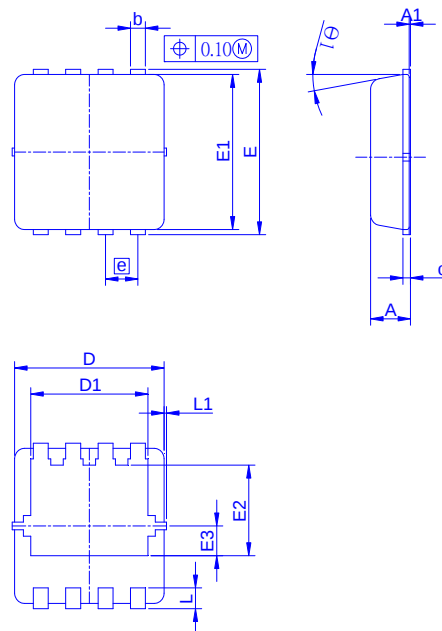
³Pulse width limited by maximum junction

temperature. **Ordering & Marking Information:**

Device Name: LB06N03B for EDFN 3 x 3



Outline Drawing



Dimension in mm

Dimension	A	A1	b	c	D	D1	E	E1	E2	E3	e	L	L1	$\theta 1$
Min.	0.70	0	0.24	0.10	2.95	2.25	3.15	2.95	1.65			0.30		0°
Typ.	0.80		0.30	0.152	3.00	2.35	3.20	3.00	1.75	0.575	0.65	0.40	0.13	10°
Max.	0.90	0.05	0.37	0.25	3.15	2.45	3.40	3.15	1.96			0.50		12°

Recommended minimum pads

