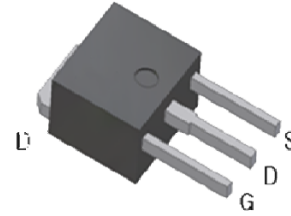


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	800V
$R_{DS(on)} (MAX.)$	3.0Ω
I_D	4A



UIS, 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^{\circ}\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 30	V
Continuous Drain Current	$T_C = 25\text{ }^{\circ}\text{C}$	I_D	4	A
	$T_C = 100\text{ }^{\circ}\text{C}$		2.5	
Pulsed Drain Current ¹		I_{DM}	16	
Avalanche Current		I_{AS}	4	mJ
Avalanche Energy	$L = 3\text{mH}, I_D = 4\text{A}, R_G = 25\Omega$	E_{AS}	24	
Repetitive Avalanche Energy ²	$L = 0.5\text{mH}$	E_{AR}	4	
Power Dissipation	$T_C = 25\text{ }^{\circ}\text{C}$	P_D	30	W
	$T_C = 100\text{ }^{\circ}\text{C}$		12	
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150	$^{\circ}\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		4.2	$^{\circ}\text{C} / \text{W}$
Junction-to-Ambient	$R_{\theta JA}$		96	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

ELECTRICAL CHARACTERISTICS (T_c = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	800			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2	3	4	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 30V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 800V, V_{GS} = 0V$			10	μA
		$V_{DS} = 640V, V_{GS} = 0V, T_J = 125\text{ }^{\circ}C$			25	
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 2A$		2.6	3.0	Ω
Forward Transconductance ¹	g_{fs}	$V_{DS} = 25V, I_D = 2A$		5		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 25V, f = 1MHz$		616		pF
Output Capacitance	C_{oss}			58		
Reverse Transfer Capacitance	C_{rss}			3.1		
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = 400V, V_{GS} = 15V,$ $I_D = 2A$		12.3		nC
Gate-Source Charge ^{1,2}	Q_{gs}			2.8		
Gate-Drain Charge ^{1,2}	Q_{gd}			3.8		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = 400V,$ $I_D = 2A, V_{GS} = 15V, R_{GS} = 10\Omega$		12		nS
Rise Time ^{1,2}	t_r			10		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			20		
Fall Time ^{1,2}	t_f			15		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _c = 25 °C)						
Continuous Current	I_S				4	A
Pulsed Current ³	I_{SM}				16	
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			1.5	V
Reverse Recovery Time	t_{rr}	$I_F = I_S, di_F/dt = 100A / \mu S$		0.6		μS
Reverse Recovery Charge	Q_{rr}			2.8		nC

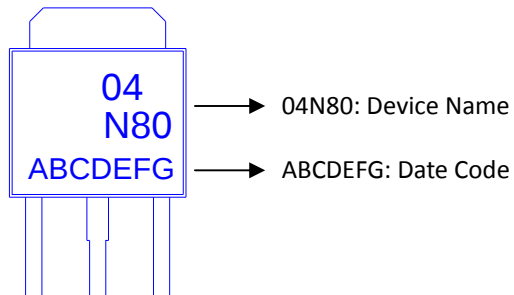
¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

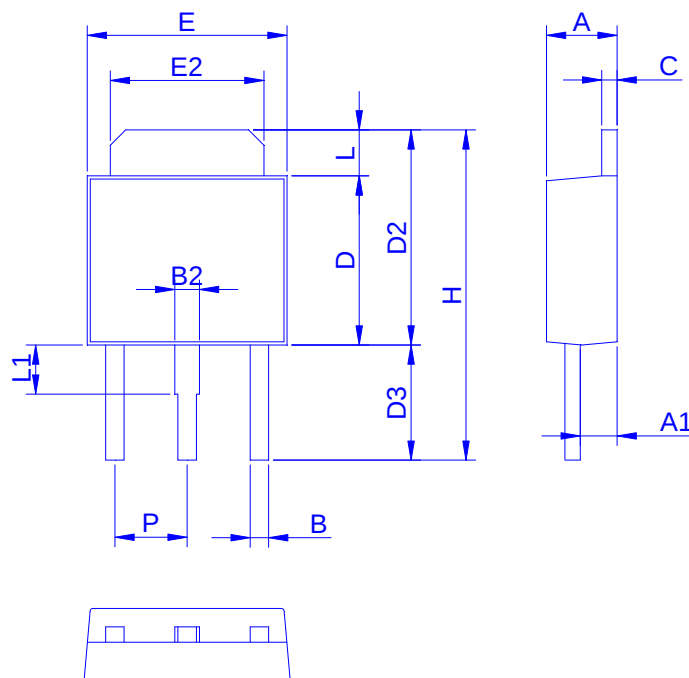
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: LB04N80E for IPAK (TO-251)



Outline Drawing



Dimension in mm

Dimension	A	A1	B	B2	C	D	D2	D3	E	E2	H	L	L1	P
Min.	2.10	0.90	0.40	0.60	0.40	5.30	6.70	3.40	6.30	4.80	10.2	0.89	0.90	2.10
Max.	2.50	1.50	0.90	1.15	0.60	6.25	7.30	4.30	6.80	5.50	11.5	1.40	1.80	2.50

TYPICAL CHARACTERISTICS

