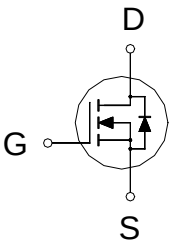
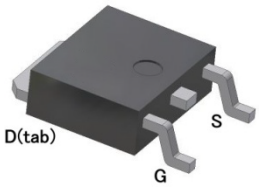
N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	650V
$R_{DSON\ (MAX.)}$	2.75Ω
I_D	4A





UIS, 100% Tested

Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current	T_C = 25 °C	I_D	4	A
	T_C = 100 °C		2.5	
Pulsed Drain Current[1]		I_{DM}	16	
Avalanche Current		I_{AS}	3	
Avalanche Energy	L = 3mH, I_D=3A, R_G=25Ω	E_{AS}	13.5	mJ
Repetitive Avalanche Energy[2]	L = 0.5mH	E_{AR}	2.25	
Power Dissipation	T_C = 25 °C	P_D	30	W
	T_C = 100 °C		12	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		4.2	°C / W
Junction-to-Ambient	$R_{\theta JA}$		110	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	650			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	2	3	5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±30V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 650V, V_{GS} = 0V			10	μA
		V_{DS} = 520V, V_{GS} = 0V, T_J = 125 °C			25	
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 2A		2.3	2.75	Ω
Forward Transconductance[1]	g_{fs}	V_{DS} = 25V, I_D = 2A		2		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		475		pF
Output Capacitance	C_{oss}			50		
Reverse Transfer Capacitance	C_{rss}			3.2		
Total Gate Charge[1,2]	Q_g	V_{DS} = 300V, V_{GS} = 10V, I_D = 2A		8.6		nC
Gate-Source Charge[1,2]	Q_{gs}			2.4		
Gate-Drain Charge[1,2]	Q_{gd}			2.3		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = 300V, I_D = 1.5A, V_{GS} = 10V, R_G = 20Ω		20		nS
Rise Time[1,2]	t_r			35		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			20		
Fall Time[1,2]	t_f			40		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				4	A
Pulsed Current[3]	I_{SM}				16	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			1.4	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100A / μS		0.3		μS
Reverse Recovery Charge	Q_{rr}			1.0		μC

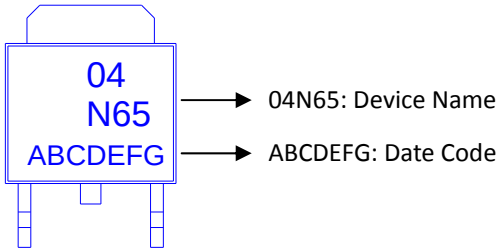
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

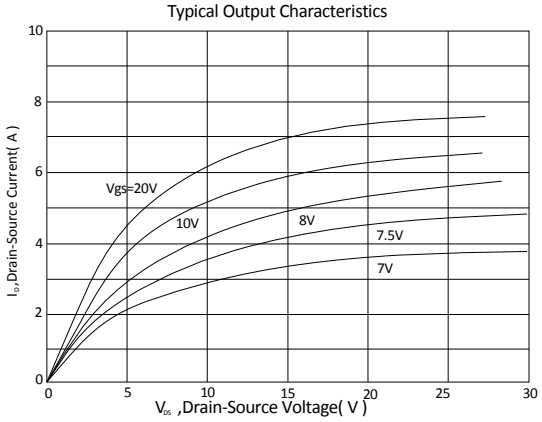
Ordering & Marking Information:

Device Name: LB04N65D for DPAK (TO-252)

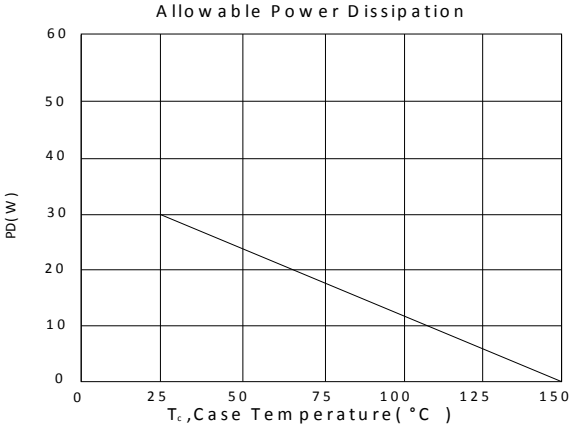


TYPICAL CHARACTERISTICS

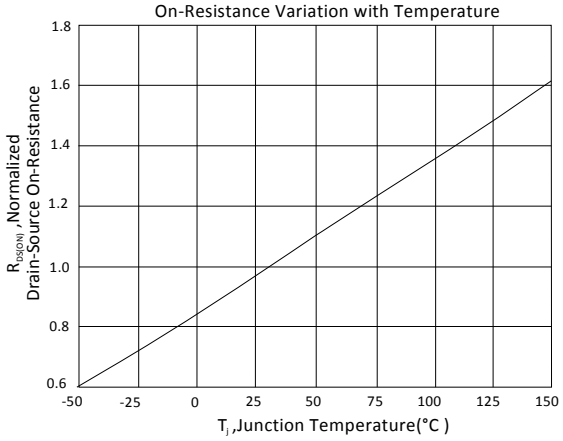
Typical Output Characteristics



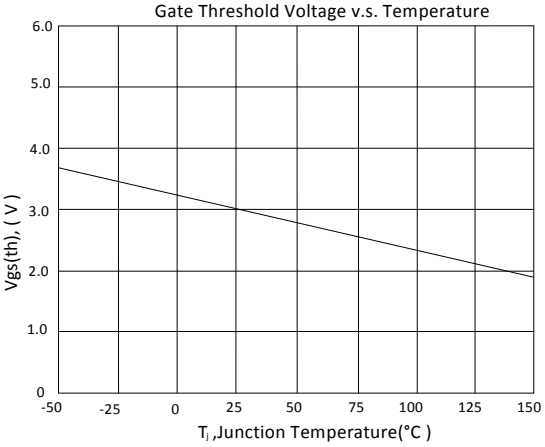
Allowable Power Dissipation



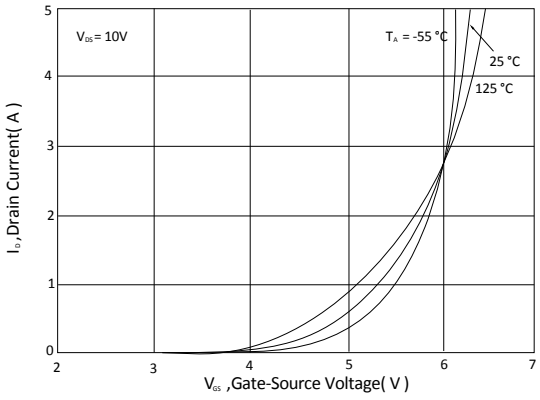
On-Resistance Variation with Temperature



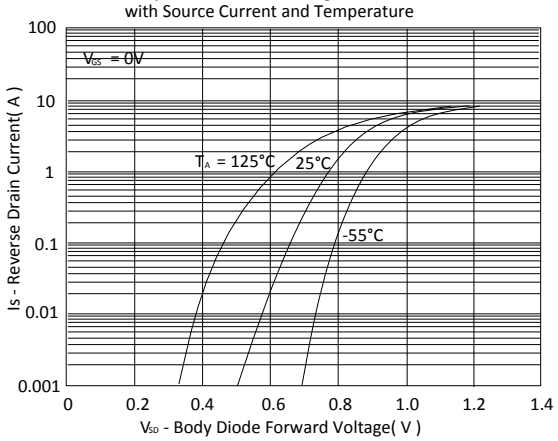
Gate Threshold Voltage v.s. Temperature

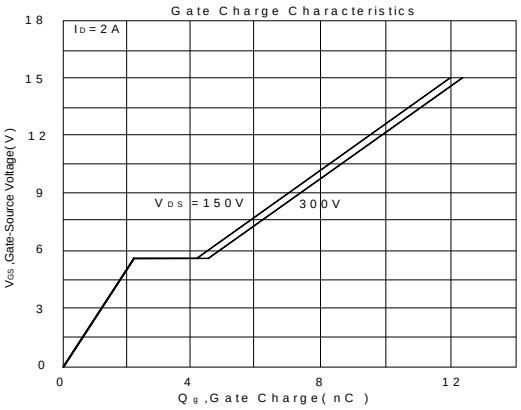


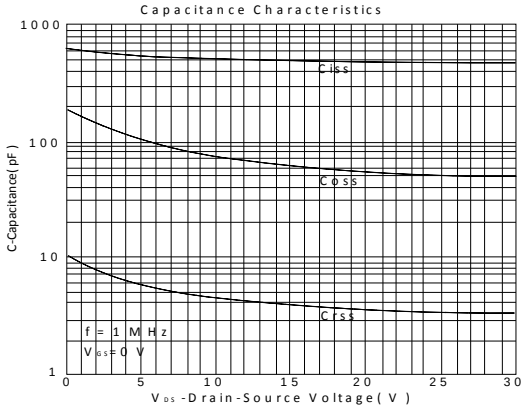
Transfer Characteristics

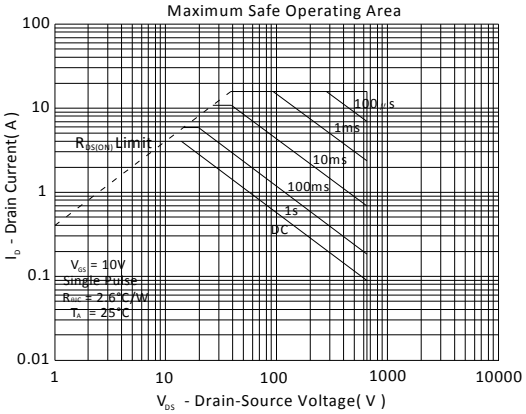


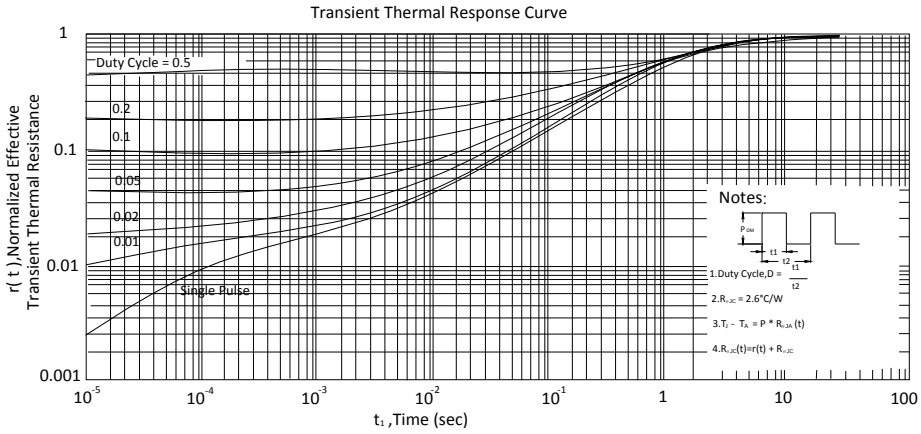
Body Diode Forward Voltage Variation
with Source Current and Temperature



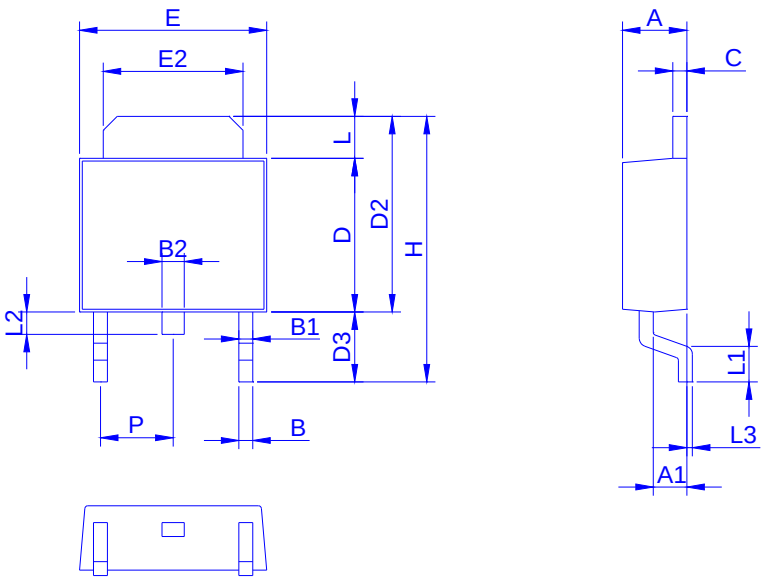

Gate Charge Characteristics
I D = 2 A
V D S = 1 5 0 V
3 0 0 V
V GS ,Gate-Source Voltage(V)
Q g ,Gate Charge(nC)


Capacitance Characteristics
C iss
C oss
C rss
f = 1 M Hz
V GS = 0 V
C-Capacitance(pF)
V DS -Drain-Source Voltage(V)


Maximum Safe Operating Area
100 μs
1ms
10ms
100ms
1s
DC
R DS(ON) Limit
V GS = 10V
Single Pulse
R θJC = 2.6°C/W
T A = 25°C
I D - Drain Current(A)
V DS - Drain-Source Voltage(V)


Transient Thermal Response Curve
Duty Cycle = 0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
Notes:
1.Duty Cycle,D = t1/t2
2.R θJC = 2.6°C/W
3.T J - T A = P * R θJA (t)
4.R θJC(t)=r(t) + R θJC
r(t),Normalized Effective Transient Thermal Resistance
t 1 ,Time (sec)

Outline Drawing



Dimension in mm

Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	0.95	0.30	0.40	0.60	0.40	5.30	6.70	2.20	6.40	4.80	9.20	0.89	0.90	0.50	0.00	2.10
Max.	2.50	1.30	0.85	0.94	1.00	0.60	6.20	7.30	3.00	6.70	5.45	10.15	1.70	1.65	1.10	0.30	2.50

Footprint